Semiconductor Engineers in a Global Economy

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Contents

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1. The Changing Nature of Semiconductor Engineering Work

The evolution and globalization of technology dominates the forces affecting the nature of engineering work in the semiconductor industry. U.S. semiconductor and related (EDA and equipment) firms are in many cases leading these changes both at home and abroad. With increased global competition, U.S. chip engineers must continually upgrade their skills, handle mobility among employers, and rely upon their own resources, rather than their employers, to manage their careers. The new sources of global competition do not seem to be large enough to undermine the positive employment and wage effects of the industry's continued growth for many workers, although older workers and those at the bottom of the job distribution have suffered deteriorating job opportunities. Many overseas companies, such as Taiwan's foundries and India's design services providers, are complementary to U.S. activities and have lowered barriers to entry at a time when the costs of design and manufacturing are skyrocketing. This plays to U.S. engineering strength by keeping the fabless start-up system for bringing innovation to market viable. The cost reductions enabled by Asian suppliers of fabrication and design services also help maintain the fall in price per transistor, which supports continued expansion of semiconductor markets, both at home and abroad.

The semiconductor (or integrated circuit, IC, or chip) industry involves three distinct stages of production, which have been affected differently by globalization and offshoring:

> Design: The design of integrated circuits is carried out primarily by engineers. The offshoring of this activity to low-cost locations has been accelerating since the mid-1990s.
>
> Fabrication: Wafer fabrication uses a large number of process and equipment engineers, who account for approximately 25% of total direct workers at a manufacturing or fabrication facility (called a “fab”). Offshoring and onshoring of IC factories appears to have reached a relatively mature and stable stage.
>
> Assembly and packaging: The final stage of IC manufacturing is the most labor-intensive, with engineers making up only 6% of the typical assembly plant’s workforce. Assembly offshoring began in the 1960s, and assembly has been almost completely offshored from the United States. We will ***not*** be discussing assembly in this paper because of its insignificant implications for US engineers.[1]

The semiconductor industry produces a heterogeneous output ranging from relatively simple discrete diodes and transistors all the way to complex “systems on a chip.”. Most market statistics reported here and elsewhere reflect “merchant” semiconductor sales, those sold to unrelated companies. There is a less visible share of the industry devoted to “captive” chip design and manufacture (internal to the company).

[1] For an analysis of the globalization of assembly, see Brown and Linden (2006).

This model is most prevalent in Japan, but still exists in the U.S., primarily at IBM, where nearly 50% of chip output in 2000 was for captive use.[2] Other systems companies, such as Apple Computer or Cisco that don't make or sell chips, may nevertheless design them for internal use. These chips may or may not be counted in merchant data depending on whether they are manufactured by a branded ASIC company such as LSI Logic (which would be counted) or by a manufacturing services "foundry," such as Taiwan Semiconductor Manufacturing Corporation (which wouldn't, since all foundry sales are excluded to prevent double counting).

Over the past decade, the work of engineers who design, manufacture, and market chips has been transformed by the continuous progression of manufacturing technology, which has evolved for more than 30 years along a trajectory known as "Moore's Law," the name given to a prediction made in a 1965 article by Gordon Moore, who a few years later would go on to co-found Intel. Moore's predicted that the number of transistors that can be manufactured in a given area of silicon would rise exponentially

This increase in integration has been made possible by miniaturization that is reaching the molecular level. The shrinkage of "linewidths" (the size of the smallest feature on a chip) from two microns in 1980 to less than a tenth-micron (100 nanometers) a quarter-century later. To give an idea of the scale involved, the width of a human hair is about 100 microns, and the width of a molecule is about one-thousandth of a micron (1 nanometer).

This progress has involved considerable R&D expense, and the cost of each generation of factories has steadily increased. By 2003 the price tag for a fab of minimum efficient scale had become more than $3 billion.

The Moore's Law trajectory has led to growing complexity of the industry's most important chip designs. A chip like Intel's Pentium 4, with 42 million transistors on a 180nm linewidth process, engaged hundreds of design engineers for the full length of the five-year project.[3] Design teams can also be as small as a few engineers, and project duration varies from months to years. Team size depends on the complexity of the project, the speed with which it must be completed, and the resources available.

The increase in functional integration has reached a point where certain chip encompass most of the individual elements that populated the circuit board of earlier systems, giving rise to the name "system on a chip" (SOC). SOC integration offers benefits of speed, power, reliability, size and cost relative to the use of separate chips.

Although the manufacturing cost of an SOC is smaller than that of the separate components it replaces, the fixed costs of a complex design can be significantly higher. System-level integration has drawn chip companies into software. One reason is that system software should be generated in parallel with the system-level chip for reasons of coherence. Chip companies are also offering software development environments and even applications to help differentiate their chips. Software can now account for half the engineering hours involved in a large chip development project.

U.S. chip companies account for about half the industry's revenue in 2005, with Intel alone commanding about 20 percent of the market. The only U.S.-based firm in the

[2] IC Insights data reported in Russ Arensman, "Big Blue Silicon," Electronic Business, Nov.2001.
[3]. "Comms held Pentium 4 team together," EE Times, November 1, 2000. "Linewidth" refers to the size of the features etched on a wafer during the fabrication process. Each semiconductor process generation is named for the smallest feature that can be produced.

global top ten is Texas Instruments, but the U.S. has a great many mid-size companies that account for about half the places in the top 50. Some of these are "fabless" companies that design and market chips but leave the manufacturing to other companies. All new entrants to the chip industry in recent years have adopted the fabless model.

Fabless revenue has grown much faster (compound annual growth rate of 20%) than the semiconductor industry as a whole (CAGR of 7%) over the last ten years. The largest fabless companies, Qualcomm, Broadcom, and Nvidia, had more than $2 billion each in 2005 revenue.

This paper discusses how the labor market for semiconductor engineers, both domestically and worldwide, has been changing in response to the changes in skill demands. It is based on our ongoing interview-based research on the globalization of the semiconductor industry. Since the early 1990s, the Berkeley Sloan Semiconductor Program has collected data at semiconductor companies globally[4]. As part of the on-going Semiconductor Program, during the past seven years the authors have interviewed managers and executives at dozens of semiconductor companies (both integrated and fabless) in the US, Japan, Taiwan, India, China, and Europe. In this analysis of industry and labor market trends and dynamics, we also use data from the Bureau of Labor Statistics, the Semiconductor Industry Association, and the Institute of Electrical and Electronic Engineers, as well as other published and proprietary sources (e.g., industry consultants).

We begin by looking in detail at various data sets on employment and earnings of U.S. semiconductor engineers, H-1B workers, and overseas engineers. The following section looks at overseas fabrication and design by U.S. semiconductor firms and its implications for U.S. engineers. The final section considers the outlook for the U.S. chip industry's workforce.

2. Labor Market for Engineers in the United States and Selected Countries

During the past six years, the many forces affecting the semiconductor industry include the severe recession during 2001, the recovery that stalled in 2004, the large decline in venture funding for start-ups that is only beginning to pick up, changes in the number of H1-B visas, and a drop and then recovery in foreign student applications to U.S. graduate engineering schools since 9-11. It is difficult to disentangle any underlying long-run trend in the offshoring of engineering jobs from these changes in government policies and the swings of the business cycle. This caveat should be borne in mind during the following analysis of the U.S. labor market for semiconductor engineers as well as in the discussion of engineering jobs in selected countries.

Because of the complexity of the situation, we analyze multiple data sources on U.S. semiconductor engineers, with results that are not entirely consistent. We also look at the recent data on the industry's use of H-1B visa holders.

A final section looks at the available data on engineers in selected Asian countries, with comparisons to the U.S. We detail the central role of U.S. graduate schools in training advanced foreign engineers.

[4] The Competitive Semiconductor Manufacturing program is a multi-disciplinary study of the semiconductor industry established in 1991 by a grant from the Alfred P. Sloan Foundation with additional support from the semiconductor industry. Further details are available at esrc.berkeley.edu/csm/ and iir.berkeley.edu/worktech/.

2.1 Engineering Employment and Earnings in the U.S.

To identify trends in the employment and earnings of semiconductor engineers, we use two major national data sets that have different strengths and weaknesses. The Bureau of Labor Statistics' Occupation Employment Statistics data (obtained online at www.bls.gov/oes/home.htm) provide a large sample collected from establishments that provide detailed occupation and industry characteristics. However comparison of data across years is not exact, since OES is designed for cross-section comparisons and not for comparisons across time.[5] Also educational characteristics are not given. The American Community Survey (ACS) (http://www.census.gov/acs/www/), which is a relatively new household survey that began in 1996 in order to update the Census between decennial surveys, provides detailed occupation and industry characteristics as well as education, and so it is much better suited for our labor market analysis. However the sample size is not adequate for detailed analysis until 2002 and later years. For this reason, we look at both the OES and ACS data sets in our analysis below. These two data sets yield somewhat different results, and this indicates that one should not draw strong conclusions based upon only one of the data sets.

We also describe semiconductor career paths and firm job ladders over the 1992 to 2002 period by using the very large Census LEHD data set that links employees and employers, in order to look at how workers form their career paths by piecing together the jobs offered by semiconductor firms.

2.1.A Employment and Earnings of U.S. Engineers

We begin our discussion of semiconductor engineering jobs in the U.S. by looking at employment and annual earnings for selected engineering jobs in 2000 and 2005 from in the OES. For the semiconductor industry, we use the North American Industry Classification System (NAICS) "Semiconductor and Other Electronic Component Manufacturing" (NAICS four-digit level 3344), which includes relatively low-value components such as resistors and connectors. The most relevant subcategory, "Semiconductor and related device manufacturing" (NAICS 334413), accounted for 39% of employees (and 45% of non-production workers) in the 3344 category in 2003, but occupation-specific data are not available at this level of industry detail.[6]

Nationally in 2005, 2.4 million people were employed in "engineering and architecture" occupations[7], where their average annual earnings were $63,920 (see Table 1). Another 2.9 million people were employed in "computer and mathematical" occupations, where their average annual earnings were $67,100. National employment in engineering and architecture fell 7.5% from 2000 to 2005, and average annual earnings of these workers rose 18.2% (more than the CPI-urban, which rose 13.4%[8]). Computer and

[5] The OES survey methodology is designed to create detailed cross-sectional employment and wage estimates for the U.S. by industry. It is less useful for comparisons of two or more points in time. Because of changes in the occupational, industrial, and geographical classification systems, changes in the way data are collected, changes in the survey reference period, and changes in mean wage estimation methodology, as well as permanent features of the methodology. More details can be found at http://www.bls.gov/oes/oes_ques.htm#Ques27.
[6]. U.S. Census Bureau, "Statistics for Industry Groups and Industries: 2003", Annual Survey of Manufactures, April 2005.
[7] This is the broad occupational category used for engineers in the OES.
[8] http://data.bls.gov/cgi-bin/surveymost?cu

mathematical jobs increased slightly (0.7%) from 2000 to 2005, and average annual earnings of these workers rose 15.6%, slightly more than inflation.

The semiconductor industry (NAICS 3344) employed 450,000 workers in 2005, with 21% in engineering and architecture occupations (of which 36% are technicians or drafters) and 6.4% in computer and math occupations (of which 40% are support or administrators). These two occupation groups exclude managers, who are 8.2% of employment. However only 12% of electronics engineers, 7.3% of electrical engineers, 18% of computer hardware engineers, 5.8% of industrial engineers, and approximately 2% of computer software engineers (applications and systems) are employed in the semiconductor industry. Together these six occupations account for 54% of engineering jobs in the semiconductor industry, or 85% of engineering jobs if techs, drafters, and computer support occupations are excluded.

As Table 1 shows, engineering jobs ("architecture and engineering occupations") in the semiconductor industry fell a surprising 28% between 2000 and 2005[9]. However when we look at the major categories for semiconductor engineers, we see that jobs increased for electrical engineers (6%), electronic engineers (11%), and computer hardware engineers (141%), while jobs for industrial engineers fell 12%, which is the only specialty where job growth for semiconductor engineers was lower than for engineers nationally.

As suggested by the earlier discussion of system-level chip design, jobs for software engineers ("computer and mathematical occupations") in the semiconductor industry grew 6% between 2000 and 2005, while they grew less than 1% nationally. The growth was unevenly distributed, however. Semiconductor industry jobs for software applications engineers grew 40% while jobs for software systems engineers fell 14%.

On average, engineers ("architecture and engineering" occupations) in the semiconductor industry command a higher salary than their counterparts in other industries. In 2005, semiconductor industry engineers earned 7.5% more than engineers nationally, and software engineers ("computer and mathematical" occupations) in the semiconductor industry earned 16% more than software engineers nationally. For a given specialty, engineers in the semiconductor industry received average annual earnings that were anywhere from 3% higher (for electronic engineers) to 9% higher (for computer software engineers, applications) than engineers in other industries. The six semiconductor engineering specialties all experienced average real earnings growth (i.e., above the inflation rate of 13.4% for the period), with real growth ranging from 1.9% for industrial engineers to 14% for computer hardware engineers. Note that these comparisons are not adjusted for education or experience, which we consider in the next section using a different data set.

[9] Comparison of 2000 and 2005 is not exact because SIC 367 was used in 2000 for the industry code and NAICS 334400 was used in 2005.

Table 1: Engineer Employment and Earnings, 2000 and 2005

	2000		2005			
	Employment	Avg Annual Earnings	Employment	Avg Annual Earnings	% Change in Employment	% Change in Earnings
Architecture and engineering occupations (total)	2,575,620	$54,060	2,382,480	$63,920	-7.50%	18.24%
Arch and eng occ in SC	132,150	$52,100	95,520	$68,720	-27.72%	31.90%
Electrical engineers (total)	162,400	$66,320	144,920	$76,060	-10.76%	14.69%
Electrical eng in SC	10,050	$69,560	10,620	$82,400	5.67%	18.46%
Electronic engineers (total)	123,690	$66,490	130,050	$79,990	5.14%	20.30%
Electronic eng in SC	14,170	$65,400	15,700	$82,430	10.80%	26.04%
Aerospace Engineers (total)	71,550	$69,040	81,100	$85,450	13.35%	23.77%
Chemical Engineers (total)	31,530	$67,160	27,550	$79,230	-12.62%	17.97%
Civil Engineers (total)	207,080	$58,380	229,700	$69,480	10.92%	19.01%
Computer Hardware Engineers (total)	63,680	$70,100	78,580	$87,170	23.40%	24.35%
Hardware eng in SC	5,990	$70,780	14,440	$89,870	141.07%	26.97%
Industrial Engineers (total)	171,810	$59,900	191,640	$68,500	11.54%	14.36%
Industrial eng in SC	12,580	$64,420	11,030	$74,250	-12.32%	15.26%
Mechanical Engineers (total)	207,300	$60,860	220,750	$70,000	6.49%	15.02%
Computer and Mathematical Occupations (total)	2,932,810	$58,050	2,952,740	$67,100	0.68%	15.59%
Computer and math occ in SC	27,080	$66,660	28770	$77800	6.24%	16.71%
Computer programmers (total)	530,730	$60,970	389,090	$67,400	-26.69%	10.55%
Computer software eng, applications (total)	374,640	$70,300	455,980	$79,540	21.71%	13.14%
Software eng (apps) in SC	5,890	$72,680	8,250	$86,860	40.07%	19.51%
Computer software eng, systems (total)	264,610	$70,890	320,720	$84,310	21.20%	18.93%
Software eng (systems) in SC	8,280	$76,660	7,090	$90,820	-14.37%	18.47%

Of course the years between 2000 and 2005 exhibit variations in employment rather than a smooth increase. For example, applications software engineers experienced a dip in employment in 2004 after strong employment growth in 2003, and electrical and electronics engineers experienced a dip in employment in 2003 followed by very strong employment growth in 2004. This is consistent with the jump in the national unemployment rate for electrical and electronics engineers to 6.2% in 2003, as it converged for the first time in 30 years with the general unemployment rate, before falling back in 2004 to a more typical rate of 2.2%.[10]

Overall we can say that the labor market for semiconductor engineers appears to be relatively strong in the five years since the dot-com bust in 2000, when, nationally, earnings have mostly stagnated during the economic recovery, with income gains going mainly to the top decile (and especially the top 1%). Semiconductor engineers have experienced better job and earnings growth than engineers in the same specialty in other industries. Employment fell for industrial engineers and software systems engineers in the semiconductor industry during this period, but grew for the other four specialties. Although earnings growth was relatively high only for computer hardware engineers and electronic engineers in the semiconductor industry, the six specialties of semiconductor engineers have high average annual earnings, which ranged from $74,250 for industrial engineers to $90,820 for software systems engineers in 2005.

2.1.B Age-Earnings Profiles by Education

To look at the earnings structures of U.S. semiconductor engineers by education and experience, we use another data set—American Community Survey (ACS) (http://www.census.gov/acs/www/). Age-earnings profiles by three education groups (<BS, BS, MS/PhD)[11] were calculated using the ACS for the years 2000, 2002, and 2004 for a sample of workers defined as follows:

- age 21-65
- in industry code 339 (Electronic components and products, comparable to NAICS 3344 and 3346)
- in a set of occupation codes (selected electrical and electronic, software, and other engineering occupations and selected managerial occupations).[12]

The age-earnings profiles for the BS (Figure 1 and Figure 2) and MS/PhD groups (Figure 3 and Figure 4) show how the semiconductor engineer annual earnings increase with knowledge and skill, which are proxied by education and experience (age), in two years (2000 and 2004).

[10]. Data were provided by Ron Hira. BLS redefined occupations beginning with the 2000 survey covering 1999, but there is no evidence that the redefinition has contributed to the post-bubble unemployment rise. See also "It's Cold Out There", IEEE Spectrum, July 2003.

[11] <BS includes workers with a high school degree or GED but no BS degree (the proportion of this group that had did not have an associate degree was 41% in 2000, 27% in 2002 and 13% in 2004); BS includes college graduates who do not have a higher degree; MS/PhD includes workers with a Masters or PhD degree (the proportion of this group that had only a Masters was 90% in 2000, 81% in 2002 and 82% in 2004). Workers without a high school degree and workers with professional degrees (e.g., MD, DDS, LLB, JD, DVM) are excluded.

[12] We used several different samples of occupation codes in order to test for sensitivity of age-earning profiles to the definition of semiconductor engineer occupations. In the results presented here, we included SOC 172070, 172061, 151021, 151030, 151081, 172131, 172110, 172041, 119041, 113021, 111021, 112020, 113051, and 113061. When we restricted the sample to fewer occupation codes, the age-earnings profiles remained mostly stable, with the earnings of the top 10% increasing for older groups with the inclusion of more managerial occupations.

Figure 1: 2000 Age-Earnings Profile, BS Holders

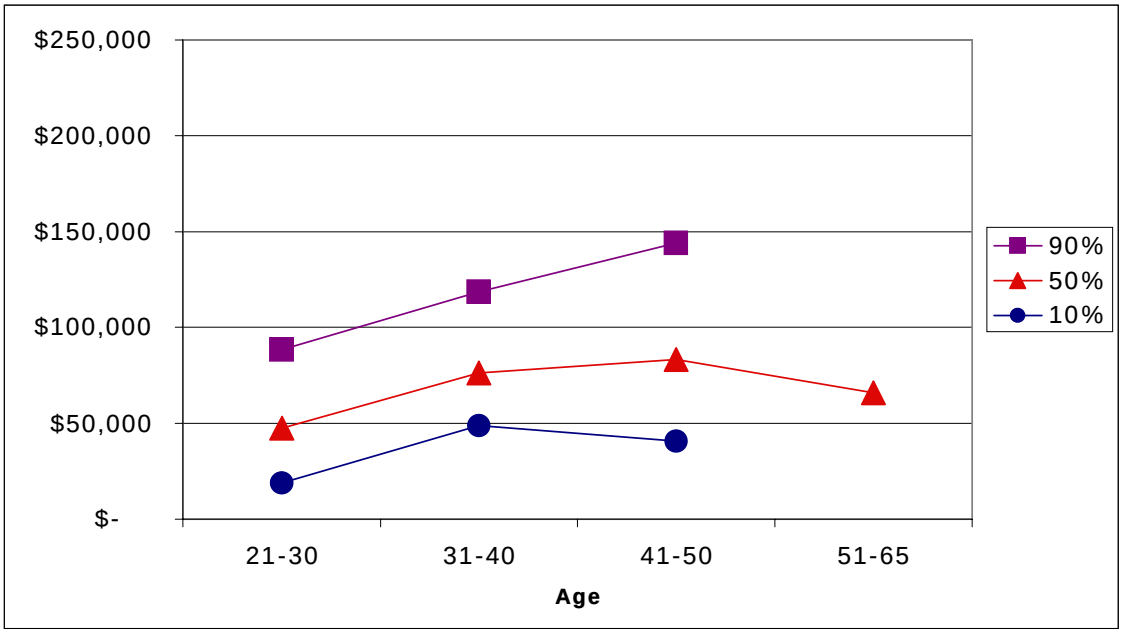


Figure 2: 2004 Age-Earning Profile, BS Holders

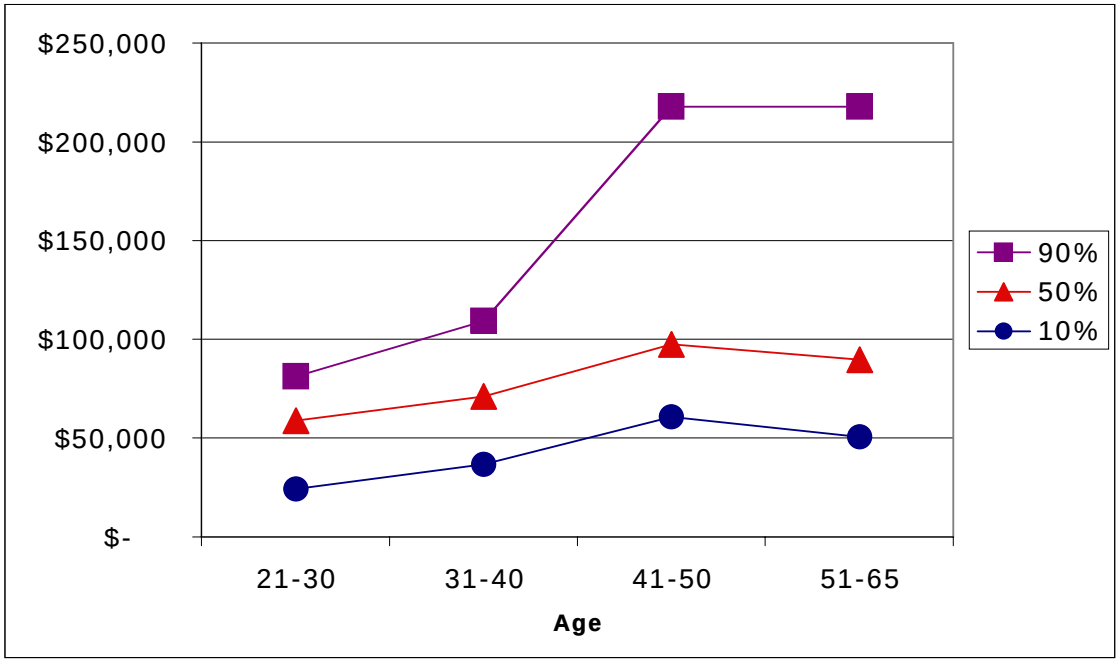


Figure 3: 2000 Age-Earnings Profile, MS and PhD Holders

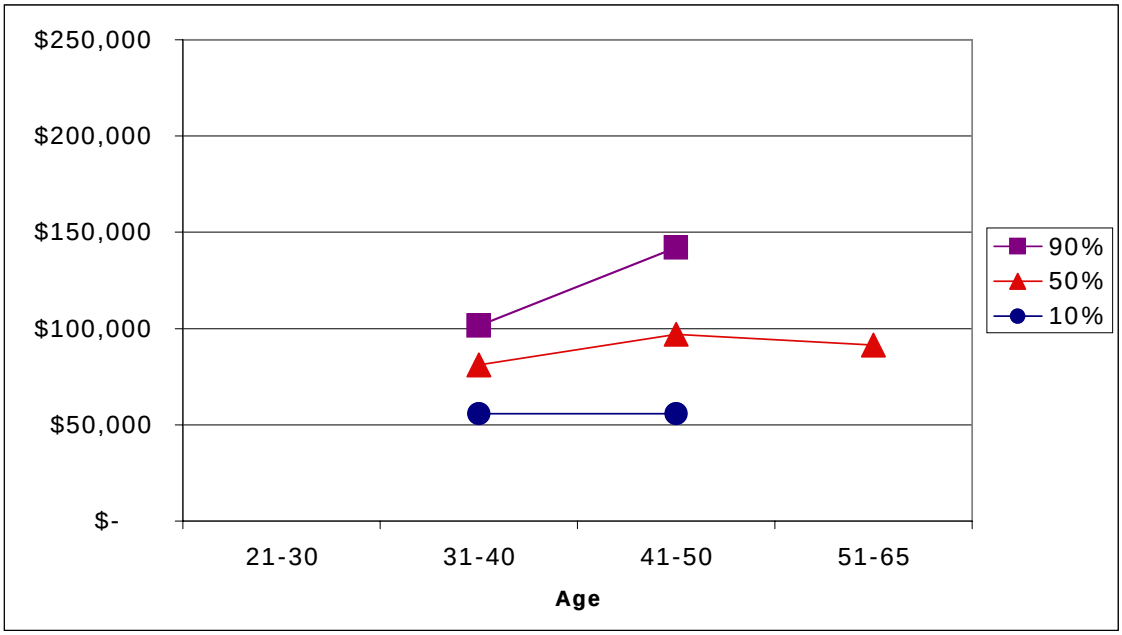


Figure 4: 2004 Age-Earnings Profile, MS and PhD Holders

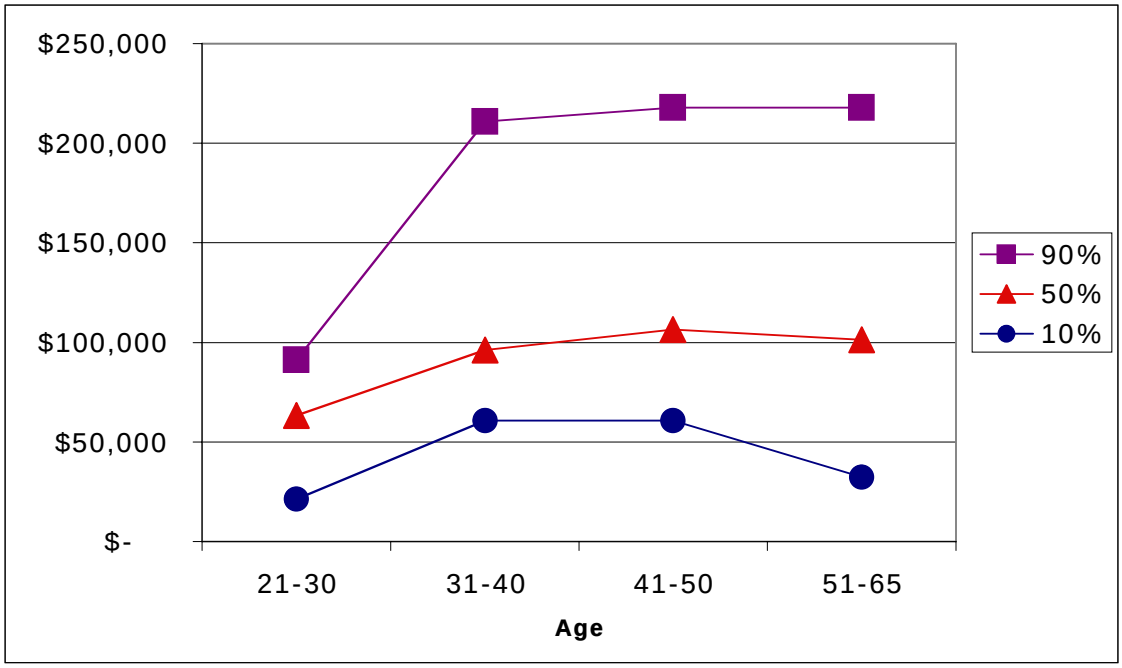


Table 2: Age-Earnings Profile (Inflation Adjusted)*

		2000				2002				2004			
		21-30	31-40	41-50	51-65	21-30	31-40	41-50	51-65	21-30	31-40	41-50	51-65
< Bachelors degree	10%					6051	29245	23194	32270		32421	35461	34448
	50%		34966	60899	48973	48405	57481	57481	49515	40526	60790	68895	70415
	90%					90759	80675	85717	72607		121579	193513	97770
	90/10 ratio					15.00	2.76	3.70	2.25		3.75	5.46	2.84
	mean		54606	53693	70505	46649	57127	56069	52402	41612	68819	84736	64523
Bachelors degree	10%	20710	53444	44536		30496	37061	49026	32825	24316	36575	60790	50658
	50%	52052	83505	91299	72372	58239	72005	88946	70945	58763	70921	97263	89665
	90%	96867	130270	158104		95299	127066	158832	158832	81053	109421	217829	217829
	90/10 ratio	4.68	2.44	3.55		3.12	3.43	3.24	4.84	3.33	2.99	3.58	4.30
	mean	58127	89949	107758	109566	60867	79222	104635	87555	57470	76809	116220	109410
Masters or PhD degree	10%		61238	61238		61945	55062	63533	45002	21276	60790	60790	32320
	50%		89073	106331	100207	79417	90005	105888	105888	63322.5	96250	106382	101316
	90%		111341	155878		95299	137654	158832	339901	91184	210737	217829	217829
	90/10 ratio		1.82	2.55		1.54	2.50	2.50	7.55	4.29	3.47	3.58	6.74
	mean		89360	114175	121988	79769	95060	120872	127819	61167	112238	127075	124065

* The repetition of earnings in some cells, especially for the 90% group, appears to be a coincidence and not a mistake, since a check of the data indicates many workers with different education and occupation reported the same earnings, which are not top coded.

These results are also given in Table 2, which shows earnings profiles for the three education groups for 2000, 2002, and 2004 with earnings adjusted for inflation (in 2004 dollars using CPI-urban).[13] One cautionary note: the sample size for 2000 is small, and so the results for 2000 are less reliable than for the later years. Also some of the age-education groups are too small to show full results.[14]

Returns to experience. Median and average real earnings increased with experience (age) for all education groups through the prime ages, and then median (but not necessarily average) earnings declined for older workers (51-65 years). Average earnings did not decline for older workers in any education group in 2000 or for older MS/PhD workers in 2002, and median earnings did not decline for older <BS workers in 2004. The general increase and then decline in median earnings implies that the engineers typically received a return to experience until they are in their fifties and sixties, when earnings then declined for many. At least part of that decline can be explained by looking at weeks worked (Table 3). Workers over age 50 are much more likely than younger groups to work less than a full year (defined conservatively here as less than 48 weeks of paid work).

Comparing across degrees, engineers with a BS diploma typically have higher returns to experience than engineers with advanced degrees. The BS holders earned one-half to three-fourths more in their peak years (aged 41-50) compared to their entry years (aged 21-30). Engineers with a graduate degree (MS/PhD) earned one-tenth to one-fifth more in their peak years compared to a decade earlier (aged 31-40), which is shortly after their entry years since they have more schooling.

The variance in earnings increased with age for prime-aged and older engineers (see 90/10 ratio and graphs). Typically the growing variance is thought to reflect faster growing pay for the higher performers, and pay for the top earners would be expected to increase as engineers become managers. However part of the increase in variance between prime-aged and older engineers reflects a sharp drop in the pay at the bottom end, especially in 2004. These profiles indicate that many older engineers are facing declining and inadequate job opportunities.

[13] Earnings for n% represents the earnings where n% of observations are below this value and (100 – n)% of observations are above this value. Earnings for 50% represents the median.

[14] For education-age-year cells (3x4x3=36) with fewer than 10 observations, no results are shown (two cells). For cells with fewer than 20 observations (and at least 10 observations), only mean and median income and full weeks worked are shown (six cells).

The sample sizes by year and education (not age) are as follows:

	2000	2002	2004
<BS	44	129	127
BS	151	367	363
MS/PhD	78	250	271

Table 3: Proportions Working Less Than Full Year (48 Weeks), By Degree Level

2000

	Age Ranges			
	21-30	**31-40**	**41-50**	**51-65**
<Bachelors degree	***	10.00%	0.00%	35.71%
Bachelors degree	25.00%	3.28%	2.56%	10.53%
Masters or PhD degree	***	3.23%	4.55%	12.50%

2002

	Age Ranges			
	21-30	**31-40**	**41-50**	**51-65**
<Bachelors degree	14.81%	0.00%	14.89%	31.82%
Bachelors degree	13.70%	11.11%	9.24%	28.57%
Masters or PhD degree	13.33%	16.13%	3.70%	26.09%

2004

	Age Ranges			
	21-30	**31-40**	**41-50**	**51-65**
<Bachelors degree	35.71%	7.69%	3.70%	20.00%
Bachelors degree	15.85%	10.62%	9.82%	10.71%
Masters or PhD degree	25.00%	7.34%	12.35%	17.78%

*** Not shown since <10 observations.

Note: The value in each cell is the proportion of that age group with the indicated degree who worked less than 48 weeks in the indicated year.

Returns to education. As expected, median and average earnings increase with education. Comparing real median earnings for the younger groups, we see that the return to a BS degree has been fairly high, with the college graduate typically earning one-fifth to two-thirds (depending on age and year) more than those who finished high school but not college. Put another way, the typical young engineer (aged 21-30) with a BS degree made the same pay as the typical engineer without a BS but with ten years more experience (aged 31-40) in 2002 and 2004.

The graduate degree premium over a BS degree (median earnings for MS/PhD compared to BS) were not stable over the short time period shown, and so it is difficult to determine the trend for returns to graduate education. The graduate degree premium for the youngest group, when many were still in school, was 36% in 2002, and then fell to 8% in 2004. The graduate degree premium for workers in the early stage of their careers (age 31-40) was 7% in 2000, and then it shot up to 25% in 2002 and 36% in 2004, which confirms our interview-based findings that the relative demand for MS and PhD holders is increasing as a result of the growing technical complexity in manufacturing and design. For workers in their peak years (age 41-50), the graduate degree premium fell from 16-19% (2000 and 2002) to 9% in 2004. For the oldest workers, the returns to a graduate degree also feel dramatically from 38-49% (2000 and 2002) to 13% (2004). For engineers above forty in 2004, the graduate degree premium of only 10% indicates labor market problems.

The variance in earnings was higher for engineers with a graduate degree than for engineers with a BS in 2004. In both 2002 and 2004, the variances of earnings for the older engineers with BS and graduate degrees was very high, with the 90/10 ratio ranging from 4.3 to 7.6.

Earnings over time. The ACS earnings profiles (for all BS engineers) show slower growth of average earnings between 2000 and 2004 than indicated by the OES data between 2000 and 2005, primarily because the ACS earnings compared to the OES earnings are higher in 2000 and comparable in 2004 and 2005. Comparing the average earnings in all industries of electrical and electronics engineers (EE) and of computer software engineers (CS) in the two data sets, we see that in 2000, ACS reports much higher average earnings for EE and slightly lower average earnings for CS than OES reports (not shown in Tables). In 2004 ACS reports much higher earnings for both EE and CS compared to OES in 2005. In the ACS, average CS earnings grew much faster than average EE earnings, whose growth did not keep up with inflation.

Although the ACS data are developed to be compared over time, while the OES data are not, the small sample sizes of the ACS data make them less representative and less reliable than the OES data. For these reasons, we cannot say with confidence to what extent semiconductor engineering earnings have grown over the period 2000 to 2005.

Summary. Overall these earnings data indicate potential problems in the high-tech engineering market. Although the returns to a graduate degree appear to be adequate, the low returns to experience for engineers with graduate degrees make the returns to the investment in a graduate degree inadequate over the engineer's career, especially the returns implied by the 2004 ACS data. The return to the BS degree and the returns to experience appear adequate for engineers under age 50. However older workers in all three education groups experienced a troubling drop in median real earnings. The data also indicate that the variance of earnings for these high-tech engineers has been rising, partly because the earnings at the bottom of the distribution are rising very slowly or falling as the engineers age. Although the high-tech engineering labor market appears strong nationally, the data by age and education indicate that engineering jobs at the bottom end may be deteriorating and that older engineers may be encounter worsening job opportunities.

2.1.C Career Paths and Job Ladders for Semiconductor Engineers

We look briefly at how the jobs and earnings of semiconductor workers, including engineers, changed over the period 1992-2002 by using a very large linked employer-employee data set, the Census-LEHD.[15] Career paths of workers who held at least one job in the semiconductor industry during the decade are shown for prime-aged (aged 35-54) males and females in two education groups—medium (some college) and high (college graduate and above).

[15] This material is taken from the Sloan-Census project that produced the book *Economic Turbulence* by Brown et al (2006) and related papers (see www.economicturbulence.com). See book chapter 5 for an overview of firms' job ladders and chapter 6 for an overview of worker's career paths in the semiconductor and four other industries (software, finance, trucking, and retail food).

Table 4: Semiconductor Career Paths, Workers aged 35-54

		Males			Females		
		Loyalist	**Two Jobs**	**Three Jobs**	**Loyalist**	**Two Jobs**	**Three Jobs**
Medium Education	**A**	$32,500	$15,015	$12,435	$13,060	$8,130	$7,300
	B	.054	.056	.058	.039	.030	.041
	C	$55,200	$25,980	$22,080	$19,485	$11,040	$11,040
High Education	**A**	$36,015	$22,850	$18,165	$14,960	$10,115	$9,280
	B	.059	.048	.047	.044	.028	.030
	C	$64,950	$37,020	$29,230	$23,380	$13,640	$12,340

Rows for each education level are:

- A: Mean initial earnings (2005 dollars, inflated using the CPI-urban)
- B: Net annualized earnings growth rate (in log points) across the simulated career path
- C: Simulated final average earnings, 2005 dollars

Source: *Economic Turbulence* (Brown et al, 2006), Chapter 6, Table 6.1. Calculated by authors from Census LEHD data. These career paths are for all workers in all occupations in the industry, so they include engineers as well as office workers, technicians, managers, and other occupations.

Career paths. Semiconductor workers exhibit two distinct types of career paths--loyalists and job changers (see Table 4). Workers who already work for a semiconductor employer with good job ladders (high initial earnings and good earnings growth) become loyalists, i.e., they do not change jobs over the period studied. The high initial earnings provide loyalists, who typically have above-average earnings growth, with career paths that are considerably above the career paths of job changers.

Workers on inferior job ladders become job changers, since by changing jobs most workers are able to eventually end up on a relatively good job ladder. Job changers have relatively low initial earnings in a job outside the semiconductor industry, and then experience substantial earnings growth (usually 20 to 30% for younger and 10 to 20% for older workers) by taking a job in the semiconductor industry. Among job changers, two-jobbers begin with higher pay outside the industry and are able to enter the semiconductor industry sooner than three-jobbers. Although high-education three-jobbers experience healthy earnings increases when they change jobs outside the semiconductor industry, the increase is below the increase experienced when they take a semiconductor job. The overall earnings growth of two-jobbers and three-jobbers is about the same over the ten year period, so the two-jobbers usually maintain their initial earnings advantage. Although job changers usually experience higher earnings growth over the decade than the loyalist, it is not enough to offset their much lower initial earnings, and so loyalists end the period with substantially higher earnings.

Job ladders. If we look at the jobs provided by semiconductor companies, we see that large firms provide 85% of the jobs in the industry. Firm fortune matters in the job ladders offered by large, low-turnover firms, as we see by comparing those with growing employment to those with shrinking employment. *Large growing firms with low turnover* provide 50% of the jobs in the industry, and these firms are usually known for providing good jobs. Semiconductor jobs tend to last relatively long in these firms, where 27% of the jobs lasted at least five years during the decade studied. *Large shrinking firms with low turnover* provide an interesting contrast. Even though the firms are reducing employment, new hires still account for 30% of jobs in semiconductors, and less than

20% of jobs have lasted over five years. These firms appear to be replacing experienced workers with less expensive new hires. A comparison of ongoing and completed long (more than five years) jobs indicates that shrinking large firms are shedding experienced workers with lower earnings growth, since earnings growth is higher (by 0.5 percentage point) in ongoing jobs than completed jobs across all groups.

In growing firms relative to shrinking firms, low- and medium-education men and all women receive much higher initial earnings (by 19 to 37%), but the men in growing firms have lower earnings growth (by -0.3 to -0.7 percentage points) while women have higher earnings growth (by 0.3 to 0.7 percentage points). High-education men have smaller differences in job ladders in growing and shrinking firms; initial earnings are slightly higher (by 7 to 11%) and earnings growth is similar (within -0.2 to 0.1 percentage points) in growing compared to shrinking firms. These results indicate that high-education men are more protected from the economic turbulence in a firm than other workers, and men's job ladders deteriorate less than those of women.

A comparison of stayers (i.e., on-going long jobs) and movers (i.e., completed 1-3 years jobs) shows that short jobs have only two-thirds of the annualized earnings growth of long jobs in both growing and shrinking large firms. Over time, growing large firms pay higher initial earnings coupled with slightly lower earnings growth, and their short job ladders have become flatter. These results indicate that growing firms use high initial earnings to attract talented workers, and then only a select group is given access to career development with long steep job ladders. Compared to growing firms, large shrinking firms pay lower initial earnings along with higher earnings growth for short jobs, and the job ladders for younger men have improved relative to older men. The trends in shrinking firms' short job ladders are consistent with market-driven employment practices.

The results indicate that large firms, both growing and shrinking, are using market- and performance-driven compensation systems. Large semiconductor firms had been known for employment practices that developed workers skills and commitment. However beginning in the mid-1980s, these established companies faced intense competition from foreign rivals and an ever-increasing pace of technological change, and they began modifying their employment and compensation practices to be more market- and performance-driven and to induce more layoffs and mobility. The growing firms appear to provide long job ladders with career development for a select group, and the other workers face either a plateau or "up or out" (although possibly those not on the fast track voluntarily leave for better jobs elsewhere). The shrinking firms appear to be selecting which experienced workers will keep their jobs, and replacing the other experienced workers with new hires at market rates. These new hires appear not to have access to long job ladders with career development, even if the long job ladders for the older workers still exist. These findings are consistent with changes we observed in large U.S. companies during fieldwork in the 1990s.

In addition to the large firms with low turnover, *small growing firms with low turnover* merit mention, since these firms are likely to be early stage fabless companies, who mainly hire technical personnel and offer relatively good job ladders for the college educated. Although these firms offer relatively low initial earnings, earnings growth is high and at the end of a decade, earnings have passed those of experienced workers in large shrinking firms and have drawn close to earnings at large growing firms with low

turnover. However the job ladders for low-educated workers (without any college) are not as good.

In general, job ladders in large semiconductor firms are superior to job ladders in small firms, job ladders in growing firms are better than job ladders in declining firms, and turnover does not mark a firm as having better or worse job ladders. Overall the economic turbulence experienced by large firms has worsened the job ladders for workers, and women's jobs deteriorate more than men's jobs. Over the decade studied, growing large firms with low turnover seem to have highly-paid new hires compete for access to long job ladders with career development, while the shrinking large firms with low turnover have experienced workers compete to keep their jobs, which are being either destroyed or filled with new hires, whose earnings reflect the market rate. Firm size and firm fortune (dynamic or shrinking) matter for workers.

Although large firms are the largest supplier of long-term job ladders in semiconductors, the importance of small and growing firms in providing excellent job ladders indicates that these firms may be an important source of good job ladders over time.

2.2 Earnings of H-1B Visa Holders in Major Semiconductor Companies

U.S. visa and educational policies have an important impact on the engineering labor force, since they directly affect the supply of engineers, especially those with advanced degrees, to the domestic market. Here we explore the earnings of H-1B visa holders, and below we discuss higher education.

The H-1B is a visa used by a foreigner who is employed temporarily in a position that requires the application of specialized knowledge and at least a bachelor's degree. H-1B visas are granted to companies (rather than workers), and the company must submit an application that provides a job title and the intended wage rate or earnings, which must reflect the prevailing wage. Prior to FY2004, employers were required to submit a $1,000 application fee. However employers often pay $1000 to expedite processing to fifteen days, as well as incur attorneys fees, so their expenses may be in the $2,500 to $8,000 range per application.[16] H-1B employees can work only for the sponsoring U.S. employer,[17] and only in the activities described in the application. A foreigner can work for a maximum of six continuous years on an H-1B visa (including one extension).

The current law limits the number of H-1B visas that may be certified to 65,000 per fiscal year, which many companies think is too low, and business has actively lobbied for higher limits. The numerical limitation was temporarily raised to 195,000 in FY2001, FY2002 and FY2003.[18] Note that only the initial application is included in the annual limitation; requests for an extension are not included. Applications by universities and nonprofit research institutions are also not counted against the cap. In addition, there are 20,000 special cap exemptions for people with Master and PhD degrees from U.S. universities. Even in 2003, before these exemptions for U.S. graduates with advanced degrees, many H-1B visa holders had advanced degrees (MS 29%, PhD 14%, Prof degree

[16] GAO (2003) http://www.gao.gov/new.items/d03883.pdf
[17] The U.S. employer may place the H-1B visa worker with another employer if certain rules are followed.
[18] http://www.uscis.gov/graphics/howdoi/h1b.htm

6%)[19] H-1Bs are granted to a wide array of occupations, including those in engineering, medicine, law, social sciences, education, business specialties, and the arts.

We collected data from the H-1B applications certified[20] to the top ten U.S. chip vendors and the top ten non-U.S. chip companies (referred to here for convenience as the top-20 companies) over the period 2001 through 2005 (U.S. government fiscal years). On the application, companies can provide either a specific proposed pay rate or the minimum and maximum of the proposed pay range, and pay can be annual, monthly, weekly, or hourly[21]. The twenty companies in our sample were granted approval of 15,784 H-1B engineering visa applications during the five years, of which 14,035 went to the U.S. firms; 49% stated a specific salary, and 51% stated a minimum and maximum salary, which we report separately in Table 5. We also look at four occupation groups, which represent most of the semiconductor applications: electrical engineering, computer-related jobs, manufacturing-related jobs, and business and administrative jobs. Here we discuss the average wage given or the average minimum of the range given. Since most H-1B applications were made by U.S. firms, we focus on these. Overall more of the applications by non-U.S firms were for business and support jobs (15%) or for non-EECS engineering jobs (18%), and the applications were more likely to state actual earnings (80%). The earnings stated by the non-U.S. companies for EE and CS applications tended to be slightly higher on average with a larger 90/10 ratio, and to be lower on average for the non-EECS jobs with a larger 90/10 ratio.

The U.S. chip companies were most likely to apply for H-1B visas for EE jobs (37% with average earnings $77,560 or average min $66,944) or CS jobs (52% with average earnings $78,537 or average min $75,685). The other applications were primarily for other engineering jobs (8% with average earnings $79,806, or average min $65,425). Applications for the EE and CS jobs show interesting differences. EE applications primarily stated the actual earnings, whose distribution tended to be approximately 15% above the distribution for the minimum rate when a range was given. In contrast, CS applications primarily stated a range, whose minimum had a distribution close to the distribution of the stated earnings.

We checked the applications by all other companies for EE and CS jobs (called "other firms" here), in order to see if they had comparable earnings, since H-1B visas might be functioning differently in different industries. Not surprisingly, the top chip companies accounted for 56% of all EE applications and only 5% of all CS applications. Interestingly the other firms mostly stated actual earnings in their H-1B applications for both EE and CS jobs. The actual earnings for EE applications in other firms have a lower mean and 10th percentile compared to the top chip firms; the actual earnings for CS applications in other firms have a considerably lower distribution compared to the top chip firms. The H-1B applications for EE-CS jobs in the chip industry appear to carry a premium compared to other industries.

[19] USCIS Report, "Characteristics of Specialty Occupations Workers (H-1B): Fiscal Yaer 2003" http://www.uscis.gov/graphics/aboutus/repsstudies/h1b/FY03H1BFnlCharRprt.pdf

[20] During this five year period, 1.6% of the applications were denied (including a small number put on hold), and these applications are not included in our analysis. We also dropped one outlier: an application stating $10.6M as the pay for a senior test engineer, with the prevailing wage given as $93,330.

[21] These two methods of applying (actual pay and range) are reported separately here. Most applications (95%) are make using annual earnings, and so monthly, weekly, and hourly pay is converted to annual using twelve months, fifty-two weeks, or 2000 hours.

If we compare H-1B pay to earnings for EE-CS engineers, we recall that EE-CS engineers earned on average $69,000 to $96,000 (overall average $86,000) during 2000 to 2004 according to ACS data, and earned $66,000 to $84,000 (overall average $74,000) during 2000 to 2005 in the OES data. The average earnings for H-1B visas granted to the top 20 semiconductor companies were between these two national averages. However it is hard to make comparisons of these earnings independent of worker experience and education, since many semiconductor companies hired their H-1B visa workers as new EE-CS graduates, often with graduate degrees, from U.S. universities.

The GAO (2003) study of H-1B visa holders compared the annual pay for a selected group of occupations, including electrical/electronic engineers (called EEs), to a sample of U.S. workers using the Census Department's Current Population Survey in 2002. As GAO notes, these annual salary comparisons are not exact for a variety of reasons, including that we do not know if the visas are actually used. In addition, the GAO appears to use data from the two-thirds of the applications that reported actual annual rate paid, which, as Table 11 indicates, may have paid lower average salaries than the applications that reported minimum-maximum rates.

The GAO comparison of EEs with H-1B visas compared to U.S. citizens in 2002 show that the H-1Bs compared to citizens are younger (32 years vs 41 years; 62% under 35 years old vs 28%) and much more likely to have graduate degrees (50% vs 20%) (GAO, 2003, pp 14, 15). When median annual salary of EEs aged 31 to 50 years old are compared, H-1Bs earned less than citizens: H-1Bs with graduate degree earned $77,000, and citizens earned $88,000; H-1Bs with less than a graduate degree earned $65,000, and citizens earned $70,000 (ibid, p 42). For younger EEs (aged 18-30) without a graduate degree, however, H-1Bs earned more than citizens ($60,000 vs $52,000; ibid, p 42). These data indicate that H-1B visa holders may be having a downward impact on the labor market opportunities of mature engineers, but probably not on young engineering college graduates.

Table 5: H-1B Visa Applications Approved, 2001-2005

Top Ten US Chip Firms						
EE Job Codes		Obs (%)	Mean	Std. Dev.	10%	90%
Rate given		3436 (24%)	77,560	16255	62,400	96,160
Range given	min		66,944	13991	52,800	85,225
	max	1792 (13%)	102,992	23410	73,375	130,000
CS Job Codes						
Rate given		2106 (15%)	78,537	18275	61,302	98,239
Range given	min		75,685	18318	56,277	100,000
	max	5234 (37%)	96,118	19662	75,000	125,000
Manufacturing Engineer Job Codes						
Rate given		649 (5%)	79,806	16801	58,200	96,000
Range given	min		65,425	14609	48,788	85,000
	max	403 (3%)	104,798	25202	73,006	130,000
Business, Marketing, Admin. Support Job Codes						
Rate given		163 (1%)	87,533	40824	50,400	130,000
Range given	min		73,549	24725	44,200	106,000
	max	252 (2%)	101,535	34193	64,900	140,000
Top Ten Non-US Chip Firms						
EE Job Codes		Obs (%)	Mean	Std. Dev.	10%	90%
Rate given		430 (25%)	80,161	18941	59,527	105,694
Range given	min		77,580	18627	55,104	99,808
	max	188 (11%)	106,911	31388	70,900	154,300
CS Job Codes						
Rate given		432 (25%)	79,525	18476	57,500	101,100
Range given	min		68,712	13843	52,361	86,606
	max	124 (7%)	91,773	22201	64,676	120,000
Manufacturing Engineer Job Codes						
Rate given		292 (17%)	73,458	16419	53,600	95,000
Range given	min	19 (1%)	69,070	16997	53,100	102,168
	max		86,217	25232	60,270	132,000
Business, Marketing, Admin. Support Job Codes						
Rate given		230 (13%)	81,882	39447	42,150	134,838
Range given	min		60,406	24271	39,145	88,486
	max	34 (2%)	82,882	36511	50,000	140,000
Other Chip and Non-Chip Firms						
EE Job Codes		Obs (%)	Mean	Std. Dev.	10%	90%
Rate given		7701 (6%)	69,302	24175	45,000	100,000
Range given	min		67,737	20807	45,000	95,256
	max	2098 (2%)	84,710	28592	50,000	124,000
CS Job Codes						
Rate given		96720 (71%)	60,698	20371	42,000	87,250
Range given	min		58,523	16860	42,000	81,600
	max	29964 (22%)	77,277	25747	50,000	120,000

Source: U.S. Department of Labor: http://www.flcdatacenter.com/CaseH1B.aspx
Note: companies can submit applications with a specific proposed rate to be paid, or provide a range (min, max). No duplicates were submitted.

H-1B Visa applications for Intel and Motorola. We explore the H-1B visa applications in greater detail for two large companies (see Table 6)—Intel and Motorola—which together accounted for 47% of the H-1B applications in our sample. Motorola spun off its chip operations as an independent company, Freescale, in 2004. Here we include the applications made by Freescale with Motorola's applications, and also report Freescale's applications separately.

Table 6: H-1B Visa Granted to Intel and Motorola/Freescale, 2001-2005

Intel

Variable		Obs	Mean	Std. Dev.	Sample Min	Sample Max
Rate given		1580	$78,070.2	11656.51	45552	144482
Range given	min	1135	65,902.9	10214.89	29878	112593
	max		121,231.7	19946.58	45074	200000

Motorola and Freescale

Variable		Obs	Mean	Std. Dev.	Sample Min	Sample Max
Rate given		266	$66,435.7	28877.91	33500	375000
Range given	Min	2289	62,866.2	13117.71	27955	144753
	Max		93,186.3	31792.39	28000	1292000

Freescale

Variable		Obs	Mean	Std. Dev.	Sample Min	Sample Max
Rate given		13	$68,800.8	4826.635	58500	75000
Range given	Min	184	65,354.2	12450.58	43400	123268
	Max		99,126.1	17375.22	65200	160000

Source: U.S. Department of Labor, H-1B Program Data at http://www.flcdatacenter.com/CaseH1B.aspx
Note: companies can submit applications with ta specific proposed rate to be paid, or provide a range (min, max). No duplicates were submitted.

Intel was granted 2,696 H-1B visas (10 were not granted) during 2001-2005. Intel was more likely than the other companies in our sample to submit an earnings range rather than actual earnings. For the applications stating an actual rate, Intel's average was very close to the average for the top 20 companies. Intel's average minimum was also comparable to the top-20 average, but its average maximum was almost 20% higher. Intel applied for H-1B visas for a wide range of jobs, and the actual earnings ranged from $45,552 to $144,482 (and possibly ranged between $29,878 and $200,000). Overall the Intel rates seem to reflect the national EE-CS salaries in the ACS. However the range of earnings across job applications was extremely large and indicates that Intel was using H-1B visas to fill jobs that varied across skill and experience.

Motorola/Freescale was granted 2,521 H-1B visas (34 were not granted). Motorola differed from other top-20 companies by stating a specific proposed wage only 10% of the time, and then the average given was 16% below the average for the top-20 companies. Motorola's stated average minimum-maximum earnings were also below those of the other top 20 companies. Motorola's average minimum earnings were 4% below, and Motorola's average maximum earnings were 9% below, the top-20 average.

However note that the highest maximum-maximum wage ($1,292,000) of all the companies was requested by Motorola, and the Motorola rates seem to be slightly higher than the national EE-CS salaries in the OES.

If we compare Freescale's applications to Motorola's for the years 2004 and 2005, we can estimate to what extent the Motorola applications were for engineers in their semiconductor business. Freescale was granted 11% as many H-1B visas in 2004 and 18% as many in 2005 as Motorola. Freescale's pay rate had a much narrower range than Motorola's pay rate, with the ratio of Freescale's sample maximum to minimum rates between 2.5 and 2.7 while Motorola's ratio of sample maximum to minimum rates was between 5.0 and 46. However Freescale's averages for the minimum and maximum rates were very close to Motorola's averages in 2004 and 6% higher in 2005. This indicates that the semiconductor engineers had only average earnings compared to other jobs at Motorola, which covered a very broad range of occupations.

The proposed wages for the top-20 companies as well as for Intel and Motorola indicate that some of the H-1B visas were for high-level jobs that paid well over $100,000, as well as for low-level jobs that paid well under $50,000. To what extent the lower-paying jobs are being used to keep semiconductor earnings low for domestic new hires, and to what extent the higher-paying jobs are going to foreigners at the expense of qualified experienced U.S. engineers cannot be determined. These remain important policy questions.

Inter-year comparisons. If we compare the H-1B visas granted by year, we see that H-1B visas granted to the top-20 companies, especially to Intel and Motorola/Freescale, jumped in 2004 and remained high in 2005,even as the national H-1B limitation and fee dropped dramatically. The semiconductor companies seemed to be benefiting from the additional 20,000 H-1Bs available for workers with a graduate degree from U.S. universities. Over the five year period, 61% of the H-1B visas were awarded to the top-20 companies during the last two years, and 53% of the H-1B visas awarded to the top-20 companies were granted to Intel and Motorola/Freescale during that time.

Intel's H-1B visa policy appears to have shifted dramatically during the five year period. Intel increased its use of H-1B visas: one-quarter of the H-1Bs were granted in the first three years and three-quarters in the last two years. The company shifted from stating the min-max range to stating the actual rate in applications, although the earnings rates remained comparable.

Motorola/Freescale also increased their use of H-1B visas during the five years, with 40% granted in the first three years and 60% in the last two years. Motorola continued to primarily use the min-max rate range (rather than actual), and the rates stated remained comparable over the period.

H-1Bs as a share of workforce. Let us look at how these H-1B visa applications compare to company employment. In 2005, Intel employed approximately 99,900 people worldwide, with more than 50% locate in the U.S., and Motorola employed 69,000 employees (number of domestic employees not given)[22]. This indicates that approximately 2.6% of Intel's workers were newly-hired H-1B visa holders. If H-1B visa

[22] These employment figures are from the company's 10-k reports: Intel at http://finance.yahoo.com/q/sec?s=INTC and Motorola at http://finance.yahoo.com/q/sec?s=MOT.

holders work for Intel for at least five years, then approximately 5.4% of their domestic workers were H-1B visa holders, which translate to a larger percentage of their engineers.

H-1B visa holders were probably an even larger proportion of the workforce at Motorola, since they accounted for 3.7% of all employees worldwide. The percentage of domestic engineers that are H-1B visa holders could easily be twice that.

These data indicate that semiconductor companies use H-1B visas strategically in hiring and managing their engineering talent. Below we see that part of the reason for the importance of H-1B visas is that major U.S. universities are providing graduate training to many foreign students, and upon graduation these students are in great demand by U.S. companies.

Now let us briefly look at the engineering labor markets in selected Asian countries.

2.3. Engineering Jobs in Japan, Taiwan, China and India

A major problem with comparing semiconductor engineering talent across countries is that the engineers in China and India, and to a lesser extent Taiwan, are younger and have less education than the engineers in the U.S. and Japan. In India and China, technicians with a two-year degree are often classified as engineers, and this is much less often the case in the U.S. and Japan. India and China have very little graduate training available in semiconductor engineering, and what is available is not comparable to the graduate programs in the U.S. and Japan. Taiwan is an intermediate case, where their undergraduate and masters engineering programs are comparable to those in the U.S. and Japan, although their PhD programs are still catching up.

Taiwan's semiconductor industry was built on the backs of PhD engineers who returned after receiving their degrees and valuable work experience in the United State. We see a similar process occurring in China and India, and in many ways we think that Taiwan provides us with a model of how semiconductor engineering will develop in India and China as the semiconductor industry matures, with the important difference that Taiwan is a much smaller country. In India and China, the industry is still quite young in design, in which both countries are active, and in fabrication, which is not yet occurring in India. Subsidiaries of multinational companies (MNCs) are playing a major role in the development of the semiconductor industry in India. In China, domestic companies, often with personnel and funds from Taiwan, are playing a major role in semiconductor design. Both MNCs and domestic companies (again with input from Taiwan) are playing a major role in semiconductor fabrication in China.

Overview of engineering in Asia. With the caveat that comparisons of semiconductor engineering talent in the U.S., Japan, Taiwan, China and India is a comparison of engineers with different education and experience, we present rough estimates for engineer salaries, worldwide fab investment by local companies, and the number of active chip designers (excluding embedded software) in Table 7, which is based on a combination of published sources and interviews, We also include an index of intellectual property protection for these countries, since this is an important consideration in deciding what engineering activities to undertake in other countries. However the IP protection rating covers all industries, and so weakness may be driven by

lapses in specific sectors such as pharmaceuticals, trademark goods, or recorded media, which are not relevant to the semiconductor industry.

The salary figures suggest that engineers in the United States and Japan earn much higher pay compared to Asian engineers. These data are imprecise and have high variance; they are intended as a general guide only. The salaries are for engineers with at least five years experience in the U.S. and for engineers aged 40 in Japan, since that is the approximate age they exit the union and begin to experience greater salary increases. The semiconductor engineers in the other countries tend to be younger and less experienced, and so the salaries for China and India are for engineers with one to three years experience. As the semiconductor industry quickly expands in China and India, wages are reportedly rising rapidly. For example, the salary range offered for a design engineer with one to three years experience by SanDisk in Bangalore at jobstreet.com in June 2005 was $9,200 to $18,400 (at 43.52 Indian Rupees to the dollar).

Table 7: Statistics, Selected Countries

	Annual EE/CS engineer salary	Value of fabs constructed by country of ownership, 1995-2006	Number of chip designers	Intellectual property protection, 2002 (10=high)
United States	$ 82,000	$74 billion	45,000	8.7
Japan	$ 60,000	$66 billion	--[a]	6.2
Taiwan	$ 30,000	$72 billion	14,000	6.7
China	$ 12,000	$26 billion	7,000	4.0
India	$ 15,000	$0	4,000	4.2

[a] We have been unable to obtain an estimate for the number of chip designers in Japan.
Sources: U.S. salary from 2004 BLS Occupational Employment Statistics web site (average for electronics and software engineers in NAICS 3344); Japan salary (average for circuit designer and embedded software engineers aged 40 years old) from Intelligence Corporation's data on job offers in 2003; Taiwan salary information from March 2005 interview with U.S. executive in Taiwan; China and India salaries are estimated based on a combination of interviews, business literature and online job offerings; value of fabs (when fully equipped) from Strategic Marketing Associates (www.scfab.com), reported in "Chipmaking in the United States," Semiconductor International (www.reed-electronics.com/semiconductor), August 1, 2006; number of chip designers in U.S., China, and India from iSuppli as reported in "Another Lure Of Outsourcing: Job Expertise," WSJ.com, April 12, 2004; number of chip designers in Taiwan from interview with Taiwan government consultant to industry, March 2005; Intellectual property protection data from World Economic Forum as cited in Economic Freedom of the World, 2004 Annual Report, Chapter 3 (Vancouver, Canada: Fraser Institute). All numbers rounded to reflect lack of precision.

The salary gap is narrower for comparable key employees. One report claimed in 1999 that the salary ratio between the U.S. and India for experienced design engineers or managers was only 3-to-1.[23.] The differential between Indian and U.S. salaries has been declining as Indian salaries have been rising. The earnings of domestically-trained Indian engineers has been doubling in the first five years. Senior managers with foreign experience are paid a large premium that mostly wipes out any cost advantage, since

[23]. "Special report: India awakens as potential chip-design giant," EE Times, January 22, 1999.

these managers are critical in implementing new technology and projects.[24] I in the U.S. and Taiwan, profit sharing bonuses that vary over the business cycle can be an important part of compensation. Benefits, which include health insurance and Social Security, and options also cloud the picture in the U.S.

We also estimated the number of chip designers, since this group is critical to developing the semiconductor industry. According to some sources, the number of chip designers being added each year in India and China is on the order of 400 each.[25] However the number of chip designers can be misleading, since there is confusion about the definition of "chip designer". One industry executive claimed that the number of "qualified IC designers" in China is only 500.[26] A Taiwan consultant didn't even consider the later (and lower-skilled) stage of physical design, called "place and route," to be part of chip design;[27] this group amounts to about 30% of the Taiwan designers shown in the table.

Comparison of higher education. The United States leads the world in higher education, and especially in graduate training, as the Academic Ranking of World Universities (http://ed.sjtu.edu.cn/ranking.htm) by Shanghai JiaoTong University shows (see Table 8). Fifty-three of the top one hundred universities are located in the U.S. and five are in Japan. In the top five hundred universities, 168 are in the U.S., 34 are in Japan, and only 21 are in China, Taiwan, and India combined.

The engineering degree numbers in Table 8 must be treated with caution, since the quality of education is not comparable across countries. The numbers may indicate political and social commitment to advancing technical education rather than actual capability. Also, these numbers are dynamic because of continuing drives to expand engineering degree programs in India and especially China. According to a widely-cited Duke University study, the number of new EE-CS-IT bachelor degrees in China in 2004 had reached 350,000 (Gereffi and Wadhwa, 2005), but how long it will take the new programs to develop quality teaching programs is an open question.

Although China and India have large numbers of engineering graduates, the graduates from U.S. universities, according to our interviews, are better trained, especially in team work on projects and on tools and equipment. For example, undergraduate students in India and China usually do not have the opportunity to work on automated chip design (EDA) tools, while EE students in the U.S. do. According to McKinsey, only 10% of Chinese and 25% of Indian engineers are capable of working in the global outsourcing market (McKinsey Global Institute, 2005).[28]

[24] Interviews at fifteen semiconductor design centers in Bangalore in November 2005.
[25]. For India: "Designs on the future," IT People, February 10, 2003; for China: "China's Impact on the Semiconductor Industry," PriceWaterhouseCoopers, December 2004, p.7.
[26]. "China's Impact on the Semiconductor Industry," PriceWaterhouseCoopers, December 2004, p.7.
[27]. E-mail exchange, March 2005.
[28] These figures were arrived at by McKinsey based on a survey of HR managers at multinational subsidiaries in these and other countries which asked the question: "Of 100 graduates with the correct degree, how many could you employ if you had demand for all?"

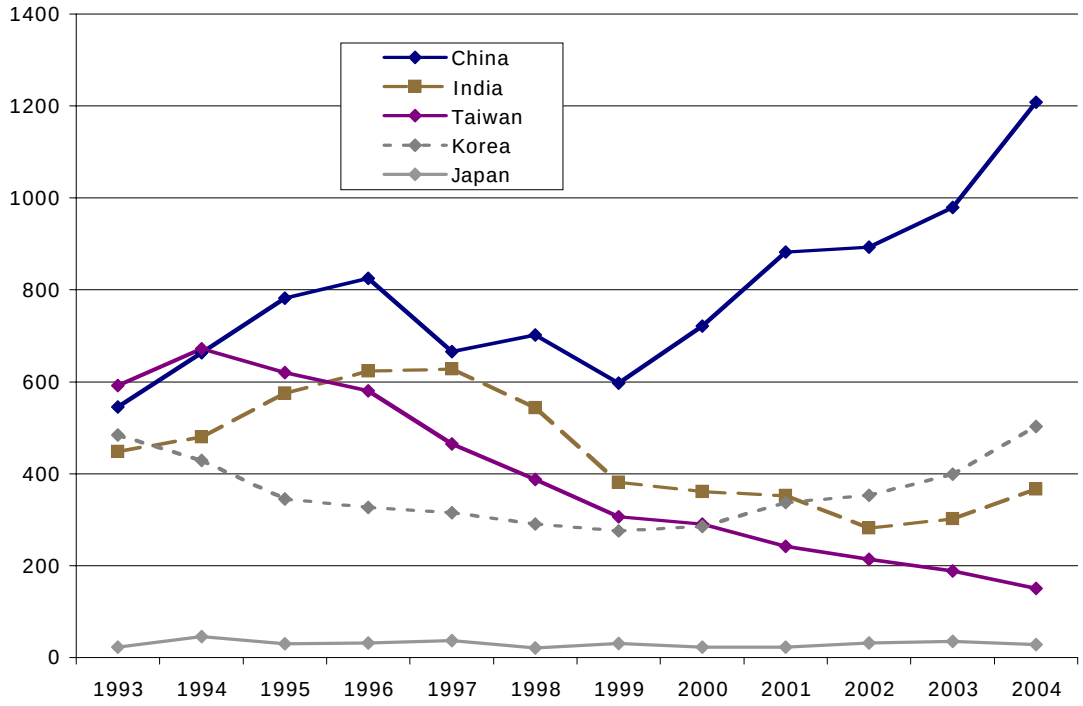
Table 8: Higher Education, Selected Countries

	2005 Academic Ranking of World Universities		Engineer BS diplomas (2001)
	Universities in Top 100	Universities in Top 500	
U.S.	53	168	110,000
Japan	5	34	110,000
Taiwan	0	5	35,000
China	0	13	220,000
India	0	3	110,000

Source: Academic Ranking of World Universities values tabulated by authors from ARWU 2005 Edition, accessible at http://ed.sjtu.edu.cn/ranking2005.htm; engineer BS degrees tabulated by authors for "Engineering" and "Math/Computer Science" from Appendix Table 2-33, "Science and Engineering Indicators 2004," National Science Foundation except for India, which is an estimate for 2003-2004 from Appendix "USA-China-India" in "Framing the Engineering Outsourcing Debate", Gary Gereffi and Vivek Wadhwa et al, Engineering Management Program, Duke University, 2005.

But the competition is not only between U.S. students trained in the U.S. and foreign students trained abroad. U.S. universities provide graduate training to many foreign students. The highest level of engineering education, the PhD, provides engineers with state-of-the-art knowledge plus the ability to conduct research and to stay abreast of the latest technology during their careers.

Figure 5: Engineering PhDs in the US by Country of Origin, 1993-2004



Source: National Science Foundation, Division of Science Resources Statistics, *Science and Engineering Doctorate Awards*:2002 (App.Table 5), 2003 (App Table 11), and 2004 (App Table 11).

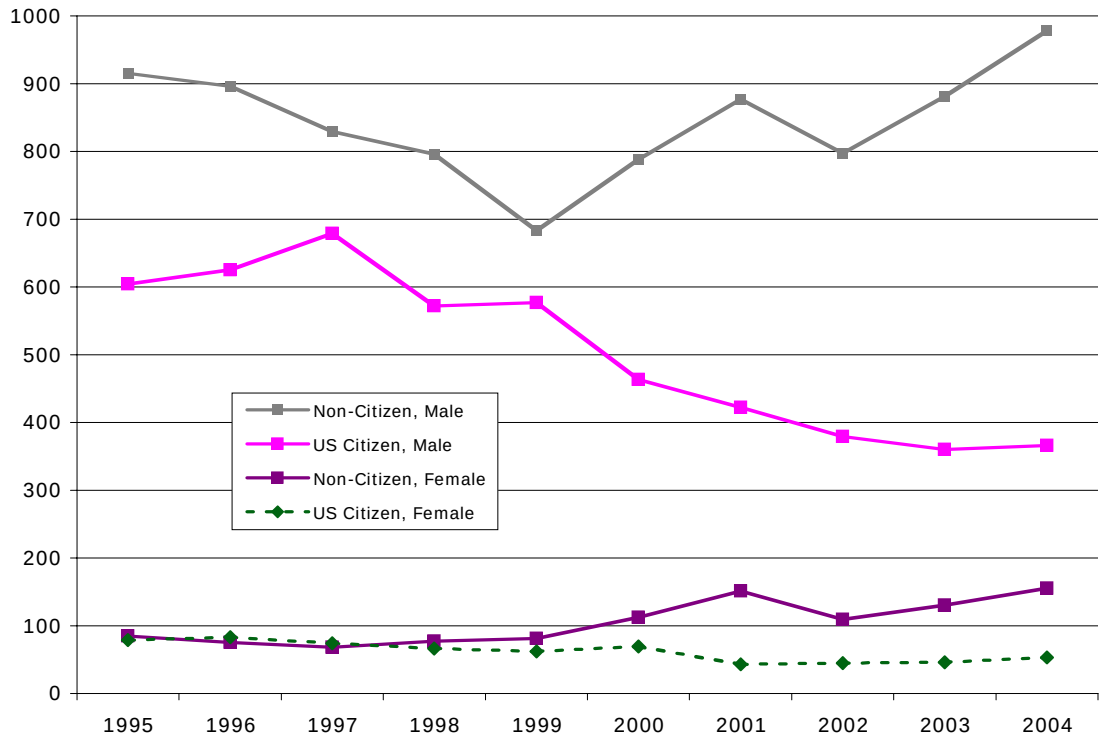
Figure 5 shows the annual engineering PhDs (not including computer science) awarded to students from five key Asian countries over a 12-year period. The figure makes clear that China has sent a large and growing number of doctoral engineers to the U.S. At the other extreme, Japan sent very few students during the period.

The number of students from Taiwan, which relied on U.S. PhDs to develop its semiconductor industry, has declined since 1994. When we were conducting fieldwork in Taiwan in February 2005, many Taiwanese semiconductor experts mentioned concerns about the decreased interest in U.S. graduate study, since Taiwanese doctoral training is considered to be inferior to U.S. training. India and Korea also sent decreasing numbers of advanced engineering graduate students in the late 1990s, although both started to increase beginning in 2002.

We also looked at the overall division of U.S. higher education resources between U.S. and non-citizen students.

Figure 6 shows a decade of electrical engineering PhDs by citizenship status and by gender. Non-citizen males garnered significantly more diplomas than their U.S. counterparts throughout the period. Non-citizen females exceeded the degrees awarded to U.S. women beginning in 1998.

Figure 6: Electrical Engineering PhDs by Gender and Citizenship Status, 1995–2004

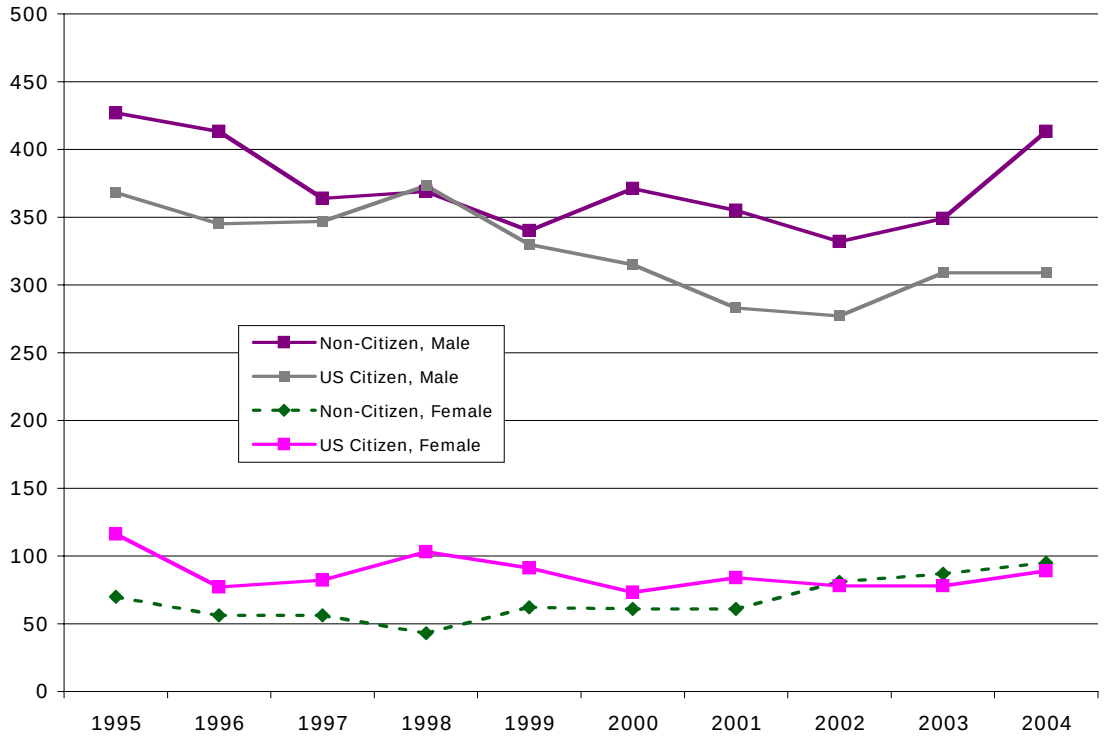


Source: National Science Foundation, Division of Science Resources Statistics, *Science and Engineering Doctorate Awards*:2004 (App.Table 3).

Turning to the same data for the field of computer science (Figure 7), the degrees awarded to citizens and non-citizens are much closer, although once again non-citizen males took home more PhDs than their U.S. counterparts in nearly every year.

These figures make clear that the U.S. is training hundreds of foreign advanced engineers every year, which augments the ability of foreign chip firms to compete with U.S. companies, as well as the ability of U.S. firms to find qualified personnel either for their U.S. operations, if the non-citizen is able to remain, or for offshore subsidiaries.

Figure 7: Computer Science PhDs by Gender and Citizenship Status, 1995–2004



Source: National Science Foundation, Division of Science Resources Statistics, *Science and Engineering Doctorate Awards*:2004 (App.Table 3).

3. Globalization of Semiconductor Engineering Activities

In this section we focus on offshoring (including global outsourcing) of wafer fabrication and IC design. First we look at the motivation for offshoring activities in the value chain, and discuss in turn the offshoring of semiconductor fabrication and IC design. Then we discuss the evolution of the design sector in these countries.

The three primary reasons for locating value chain activities globally are 1)access to location-specific resources, especially engineering talent; 2) cost reduction; and 3) local market development and access. Often, the shift of an activity to a new location via internal investment or outsourcing is in response to all three reasons. For example, a company may move chip design to China in order to take advantage of engineering talent that is low cost and knowledgeable about customized solutions for the regional Chinese telecommunication systems as well as to gain government approval for market access.

The net impact of U.S. jobs from the offshoring and outsourcing of fabrication is hard to assess. Offshore fabs have, as we will discuss below, been at least partially balanced by foreign-owned fabs in the U.S. And while Asian foundries have probably contributed to a long-run reduction of U.S. chip manufacturing, the net loss of engineering jobs has probably been offset to some extent by the increase in design jobs at fabless companies.

3.1 Fabrication and Employment

The engineering jobs in chip fabs have evolved over the last several technology generations. This is not driven so much by the miniaturization of Moore's Law (which has necessitated an increase in the diploma requirements mainly for engineers in process R&D), but rather by increases in wafer size. Larger wafers are an important tool for raising industry productivity.

From the standpoint of process and equipment engineers, a change in wafer size, which precipitates major re-engineering of the equipment and process technology, has a major impact on fab skill requirements. Here we look at how engineering work within the fab changed across the transition from 150mm to 200mm wafers, based upon detailed data gathered in the mid-90s by the Berkeley Competitive Semiconductor Manufacturing (CSM) Program at a sample of fabs running 150mm and 200mm wafers in four countries[29].

As wafer size increases, both materials handling and information systems become more automated in order to safely handle the increased weight and value of each wafer and to minimize human error. Automation changes the composition of the workforce as the need increases for engineers and declines for operators. In the CSM data, engineers increased from 15% to 24% of the total workforce between 150mm- and 200mm-generation plants, with a corresponding decline in operators from 73% to 62% (see Table 9) even as the overall employment level of the fab stayed approximately the same at about 750 workers.

Table 9: Work Force Composition

(Mean Headcount in Matched 150mm and 200mm Fabs)

	150mm	200mm
Operators	547 (73%)	470 (62%)
Technicians	91 (12%)	107 (14%)
Engineers	114 (15%)	181 (24%)
Total	752	758

Source: Brown and Campbell, 2001.

The shifting of jobs from operators to engineers resulted in the growth of higher paying, high-skilled jobs at the expense of lower paying, low-skilled jobs. However the earnings structures also changed across occupations, (see Table 10). The initial pay of

[29]. Twenty-three fabs in four countries were part of the CSM survey. For this table, the 150mm wafers fabs were matched to the 200mm wafers fabs by company, so that the company human resource policies are comparable between the two groups, which reduced the sample to fourteen.

technicians and engineers was over one-third higher in the 200mm fabs than in the 150mm fabs, and their pay premium over operators increased.

Table 10: Work Force Compensation

(Mean Wage or Salary in Matched 150mm and 200mm Fabs)

	150mm		200mm	
	Initial pay	Maximum pay	Initial pay	Maximum pay
Operators (hourly)	$5.88	$15.47	$7.12	$18.44
Technicians (hourly)	$6.68	$11.50	$9.12	$15.83
Engineers (monthly)	$1,785	$5,019	$2,381	$4,689

Source: Brown and Campbell, 2001.

A look at the returns to experience, which are proxied by the maximum pay compared to initial pay, shows that experienced engineers fared poorly as the ratio of maximum to initial pay fell from 2.8 (150mm fab) to 2.0 (200mm fab). The returns to experience for technicians and operators remained stable as the experienced techs and operators had the same pay improvement in the 200mm fab as the new hires.

The experienced engineers were losing out over time as their average maximum real salary was actually lower in the 200mm fabs compared to the 150mm fabs. In interviews, we learned that fabs liked having young engineers with knowledge of new technology, and they did not worry about losing older engineers. Over time, consequently, fabs were willing to increase wages of new hires without raising the wages of experienced engineers. Rapidly changing technology plus an ample supply of new hires and low turnover allowed the companies to flatten engineers' career ladders with no adverse consequences.

We do not have comparable data for the 300mm fab, which has total automation of materials handling and wafer processing. This was necessary because each 300mm wafer is more valuable than before, since its area is 2.25 times that of a 200mm wafer, but it is also heavier and more awkward to handle, which raises the risk of being dropped by—as well as the ergonomic risk to—human handlers.

Because these new 300mm fabs are processing advanced circuits, such as those using 90nm or 65nm processes, the amount of inspection, metrology steps, and in-line engineering-related activities are significantly higher than their older 200mm counterparts for the same wafer throughput. As a result, most of the 300mm worker savings achieved with the automation of materials handling, often cited to allow approximately 30% less labor input, is now being re-applied to the new engineering tasks, which are much higher value-added and more intellectually challenging, and include more troubleshooting. Therefore the number of workers has not been reduced as a result of the advanced factory automation; instead there has been a shift in task composition. The percentage of workers with higher engineering and technical problem-solving skills has greatly increased, while the percentage of workers needed for wafer

movement and equipment starting and stopping has greatly decreased. However the proportion of engineers has not increased.[30]

3.2 Outsourced Fabrication

The outsourcing of chip fabrication took off in the 1980s as fab processes standardized on MOS technology and the technical infrastructure for characterizing fab processes, such as BSIM models, became better-defined. In 2005, the outsourced fabrication market was worth $18 billion,[31] with most of it accounted for by dedicated contract manufacturers, known as "foundries," in Taiwan. A few integrated firms offer foundry services to help keep their fabs at full capacity. The largest of these is IBM, which had foundry sales of $832 million in addition to its own-brand chip sales of $3.5 billion

The dedicated ("pure-play") foundry model originated in Taiwan in 1987, when the government brought together investors, licensed mature production technology from the United States, and attracted Taiwanese engineers and managers with experience in the U.S. chip industry. That first foundry, Taiwan Semiconductor Manufacturing Corporation (TSMC), remains the largest in an increasingly crowded field, as shown in Table 11. TSMC was founded by Morris Chang, a Chinese-born, MIT-educated executive with 25 years' experience at Texas Instruments who moved to Taiwan in 1985.

Table 11: Top Five Pure-Play Foundries, 2005

Company (Location)	Revenue 2005 (US$ millions)	Growth (%) 2004-2005	Share of All Foundry Sales (%)
TSMC (Taiwan)	8,223	7.2	44.8
UMC (Taiwan)	2,822	-19.3	15.4
SMIC (China)	1,171	20.1	6.4
Chartered Semiconductor (Singapore)	1,132	2.6	6.2
Vanguard International (Taiwan)	354	-9.8	1.9

Source: Gartner Dataquest, Jan.2006

TSMC was large enough to have made the chip industry's top 10 list in 2005 with $8.2 billion in revenue,although foundries are excluded to avoid double-counting of their and their customers' chips. Since foundry price is about one-third of the final chip value, TSMC actually manufactured nearly $25 billion worth of chips, which would place it number two in the overall chip industry behind only Intel.

Among the top 5 pure-play foundries in Table 11, the fastest-growing is Semiconductor Manufacturing International Corporation (SMIC) of mainland China. SMIC was founded in 2000 by Richard Chang, a Taiwanese expatriate with experience in Taiwan's foundry business following a U.S. graduate education and twenty years' experience at Texas Instruments. SMIC has successfully attracted a range of technology partners and customers—primarily from the United States—hired hundreds of Taiwanese

[30]. Personal communication, April 2005.
[31] Gartner Dataquest estimate reported in "Foundry Revenue Drops in 2005, Gartner Reports," Electronic News, March 27, 2006.

engineers with foundry experience,[32] and listed its shares on the New York Stock Exchange in 2004.

Although the emergence of the foundry model in Asia meant that less production capacity would be built in the US, it has greatly facilitated the growth of the fabless design sector, which is one of the industry's growth engines, as discussed in Section 1.[33] As a back of the envelope calculation, we estimate that if all foundry production were based in the United States instead of Asia, it might add 11,000 jobs, of which some 2,600 would be highly-paid engineers.[34] But it must be noted that not all foundry sales are to U.S. customers. In 2003, for example, half of TSMC's gross revenue came from non-U.S. sources.[35]

As a point of comparison, the Fabless Semiconductor Association reported that publicly-traded fabless companies in North America employ approximately 45,000 workers as of December 2004.[36] A review of company information suggests that more than half of these are software or hardware engineers, although an unknown share of them are located offshore.

3.3 Offshore Fabrication

Offshore investments in chip fabrication were historically been driven by market access concerns, particularly tariffs, more than by cost reduction because of the capital-intensive nature of chip manufacturing. In a survey of industry executives, Leachman and Leachman (2004) found that the top five reasons, rated very close together, for fab site selection were "Tax advantages," "Supply of engineering and technical talent," "Quality of water supply and reliability of utilities," "Proximity to existing company facilities," and "Environmental permitting process and/or other regulations."[37] Empirical research on fab investment data shows that host country political institutions, the presence of other fabs, and a firm's prior investment experience also affect the location of fab investments.[38] This multiplicity of concerns surrounding such a major investment accounts for the relatively few cases of U.S.-built fabs in industrializing countries, even with the rich subsidies that have been offered by countries like Singapore. Meanwhile, foreign companies still find the U.S. an attractive place to invest, as evidenced by Samsung's recent commitment to a new, multi-billion-dollar fab in Austin.[39]

The shifts in regional markets discussed in Section 1 are reflected by striking shifts in fab capacity from the U.S. and Japan to the rest of Asia (primarily Taiwan and South Korea). In 1980, Japan and the United States accounted for 80% of fab capacity in 1980, but only 49% of capacity in 2001 (see Table 12).

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[32] "TSMC Sues SMIC," Electronic News, December 22, 2003.
[33]. see Macher, Mowery, and Hodges (1998) for a discussion of the factors leading to the U.S. industry's resurgence after its loss of global market share in the mid-1980s.
[34]. TSMC, which accounts for about half the foundry industry, has one 150mm, one 300mm, and five-and-a-half 200mm fabs outside the United States. These fabs probably have different rated capacities, but we can approximate employment by calculating 750 workers per plant, which works out to 5,625. Doubling that to approximate the entire foundry sector brings us to 11,250.
[35]. Note 27c of Form 20-F filed by TSMC with the Securities and Exchange Commission for fiscal year ended December 31, 2003.
[36]. FSA "Global Fabless Fundings and Financials Report, Q4 2004".
[37] Leachman and Leachman (2004, p. 226).
[38] Henisz and Macher (2004).
[39] David Lammers, "Analysis: Samsung fab deal ends drought for Austin," EE Times, April 14, 2006.

Table 12: Regional Location and Ownership of Worldwide Fabrication Capacity

(For each year, capacity location is shown on top and capacity ownership is shown beneath it in parentheses.)

Year	Asia ex-Japan	Europe/ Middle East	Japan	North America
1980	4% (3%)	16% (15%)	38% (37%)	42% (44%)
1990	12% (12%)	13% (9%)	45% (45%)	30% (36%)
2001	38% (39%)	13% (8%)	20% (24%)	29% (38%)

Source: Leachman and Leachman (2004), Tables 8.2, 8.4
Note: The ownership row total for 2001 adds to more than 100 because jointly owned capacity was credited in full to all owners.

However if we look at the same data in terms of region of ownership (shown in parenthesis), we see that the decline of capacity owned by U.S. companies is less severe than the fall in capacity located in the U.S. Although only 29% of fab capacity in 2001 was in the United States, U.S. companies had ownership stakes in almost 40% of global capacity. In contrast, the rise of capacity owned by companies in Asia (ex-Japan) mirrors the rise of location capacity.

Because so many fabs owned by companies in one region are located in another, these data do not directly answer the question of how much U.S.-owned capacity is located outside the United States. Rob Leachman generously helped us to make this calculation.[40] In 2001, approximately one-third of U.S.-owned capacity was located offshore as shown in Table 13. The offshore fabs were primarily in Japan and Europe, which reflects the rise of joint ventures to share risk as the cost of fabs increased. Conversely, about 22% of the fab capacity located in North America was owned by companies based in other regions (not shown).

Table 13: Distribution of North-American-Owned Fab Capacity, 2001

North America	65.4%
Europe/Middle East	18.6%
Japan	13.0%
Asia ex-Japan	3.0%

Source: Calculations courtesy of Rob Leachman.

Most fabs built today are designed to use high-capacity silicon wafers measuring 300mm in diameter. The location of such fabs provides a snapshot of where the newest, high-volume capacity is located.

[40]. The Leachman data do not include ownership shares for jointly-owned fabs. We divided such fabs by the number of regions (2 or 3) involved in ownership to estimate the U.S. share. As much as 10% of U.S.-owned capacity was in joint venture fabs in 2001, but those fabs were spread across all regions, so our estimation error is not likely to be more than 1 or 2 % up or down from the figures in the table.

As of October 2004, thirty-six 300mm fabs were in various stages of construction in addition to the twenty-four already in production (see Table 14).[41] Each of these fabs requires annual revenues of well over $1 billion to be profitable.[42] Japan and the US each have a quarter of the 300mm fab capacity, and Taiwan has a fifth.

Table 14: 300mm Fabs Producing, Equipping, or Under Construction, Oct.2004

Japan	24%
U.S.	24%
Taiwan	19%
Europe	14%
S.Korea	12%
Singapore	3%
China	5%

Source: Strategic Marketing Associates (www.scfab.com), based on theoretical full capacity and on fab location. Total adds to more than 100% because of rounding.

3.4 Design

Design outsourcing to overseas locations is still relatively limited in scale, with most of the estimated $2.5 in worldwide design outsourcing revenues being spent in the same location as the design team.[43] Many U.S. interviewees reported that they outsource physical design to small local companies on an as-needed basis. Another design function that is frequently outsourced is logic verification, the resource-intensive task of making sure that first stages of the physical implementation are a correct translation of the abstract logic. At the other extreme, architectural design, or the design of key functional blocks containing proprietary algorithms, are the least likely to be outsourced because of the risk of exposing proprietary knowledge.[44]

Outside the U.S., there are dozens of companies offering design services to help customers complete all or part of their chip designs. The largest concentrations of low-cost chip designers are in Taiwan, mainland China, and India. Because of the increasing interaction of physical design with advanced fab processes, Taiwan's foundries work closely with local design services providers such as Global UniChip (TSMC) and Faraday (UMC). In China, the emergence of low-cost foundries have also given rise to design services companies. The most advanced of these, IPCore and VeriSilicon, were both founded in 2001 by executives with years of experience in U.S. and Asia. In India, despite the lack of any significant chip manufacturing, large IT service providers such as Wipro and Tata Consultancy Services have expanded into semiconductor design services for international clients.

But the design phenomenon most likely to affect U.S. engineering jobs is the opening of offshore subsidiaries by U.S. firms, which has noticeably expanded in Asia over the last decade.

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[41]. Data from Strategic Marketing Associates (www.scfab.com).
[42]. Authors' calculation, suggested by Toshihiko Osada, based on data in Appendix 2 of Howell and others (2003). Annual depreciation and operating expense for a U.S.-based 300mm fab running 6,000 wafers per week on a 90-nanometer process totaled $975,000.
[43]. "Complex chips reignite demand for design services," EE Times, October 11, 2004.
[44]. "Outsourcing trend proves: Complex by design," EE Times, January 31, 2005, and interview, April 2004.

Offshore design investments occur for a variety of reasons and follow several different models.

Specialized skills are an important reason that U.S. semiconductor companies invest overseas, particularly in Europe. Britain, for example, has developed expertise in consumer multimedia, and Scandinavian countries are noted for their skills in wireless network technology. These specialized skill bases are often accessed by acquisition of an existing company that continues as a subsidiary. Examples abound. In 2000, Broadcom acquired Element 14, a British fabless company with 68 employees specializing in central office ADSL technology that became Broadcom UK Ltd.[45] In 2001, Agilent acquired Sirius, a Belgian designer of cellular chips for the CDMA standard with 19 employees, and made it a research and design center for next-generation cellular technology.[46] In 2005, Intel acquired Oplus, a successful maker of chips for digital television with 100 workers and that will remain an independent subsidiary.[47]

Access to markets, especially in China where the government has made direct investment a condition for access to its large and fast-growing markets, has been an important reason for offshoring development and manufacturing activities. This is less true in India, where most consumer markets are growing more slowly, but where far more U.S. firms have invested in design.

The reason for design offshoring that is perhaps getting the most attention is cost reduction. For Silicon Valley firms, some cost reduction is available by opening satellite design centers elsewhere in the U.S., where some locations have average engineering salaries that are up to 20% lower than salaries in the Silicon Valley. But these salaries are still much higher than salaries in India and elsewhere, as we showed earlier. The prospects for cost reduction offshore are better than ever because of changes in the last 20 years that have seen advances in automation, high-bandwidth infrastructure extended around the globe and the economic liberalization of large economic areas in Eastern Europe, and especially Asia,[48] although we will discuss the large array of non-salary costs associated with managing overseas operations.

Investment in low-cost locations is now part of the business plan of many new chip firms. Venture capitalists have reportedly begun to require fabless start-ups to include some offshoring of design to better leverage their resources. A typical comment is, “We don't fund chip designs that don't outsource to India. If you rely on Indian contractors for the things they do well, you can get a chip out for under $10 million. If you don't, you can't, and you won't be competitive. It's that simple.”[49] PortalPlayer, the company behind the key multimedia chip in Apple’s iPod, is a recent example of a successful start-up that set up an Indian software and chip design subsidiary within a few months of its founding in 1999.[50]

There are diverse ways that a U.S. firms can incorporate offshore design centers in its operations. Some companies value the opportunity to design on a 24-hour cycle

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[45]. “Broadcom acquires Element 14 for $600 million, enters ADSL chip market,” Semiconductor Business News, October 4, 2000.
[46]. “Agilent to buy Belgium's Sirius to offer new CDMA chip solutions,” Semiconductor Business News, May 21, 2001.
[47]. “Intel buys into consumer sector with Oplus acquisition,” Silicon Strategies, February 24, 2005.
[48]. Ernst (2004).
[49]. William Quigley, managing director at Clearstone Venture Partners (Menlo Park, Calif.), quoted in “Venture capitalist explains new rules for IC startups,” EE Times, January 16. 2003.
[50]. “Designs for Digital Audio, Auto Electronics,” Nikkei Electronics Asia, October 2002.

because of the enormous pressure to reach the market ahead of, or no later than, competitors. One established U.S. chip company adopted a rolling cycle between design centers in the United States, Europe, and India.[51] More common is the bi-national arrangement used by a Silicon Valley start-up that had all of its design beyond the initial specification done by a China subsidiary established only months after the head office was set up. Ten executives in the head office had to train the mostly inexperienced staff in Beijing, which was about thirty strong.[52] The Silicon Valley staff would review Beijing's work from the previous day then spend up to three hours on the phone (starting around 5pm California time) providing feedback and reviewing assignments for that day in Beijing. In a single-location firm, this work-feedback cycle would take two days.

Offshore subsidiaries vary widely in terms of what parts of the design chain they cover. Some subsidiaries are restricted to physical design or verification. Others may also handle logic design. In some cases, a subsidiary may be responsible for a particular type of intellectual property (e.g. 802.11 wireless blocks) or the creation of library elements. Higher-level activities like specification, architecture, and fab interface are likely to be kept closer to home. in our field research, we have noted a tendency of subsidiaries to expand their responsibilities as capabilities and trust are built up, but this is by no means universal to all subsidiaries and depends mostly on corporate strategy and, to a lesser extent, on the "entrepreneurial" abilities of the subsidiary managers.

Costs of managing offshore activities. Dividing chip designs across locations presents a number of managerial challenges, as we have learned from interviews and press reports. The sacrifice of face-to-face interaction between different parts of the design team can adversely affect productivity, and distance makes it harder to evaluate and reward individual contributions to team performance. Task assignments must be more carefully codified for offshore teams than for locally-based engineers, and managers will need to travel periodically between locations. When the separation is across borders, there are also cultural differences that can make communication less effective. An Intel engineer was reported to say that cultural differences were the single biggest problem in managing design teams between California and Israel, and this separation did not include any language differences.[53]

Cost-driven in-house offshoring incurs other costs that partially offset the difference in salaries, especially during the early stages of establishing an offshore design center. One that is often mentioned is the lower quality and productivity of inexperienced engineers. This raises monitoring costs, and offshore engineers may also require a longer training period than a U.S. team would need. Additional controls may also be needed to protect key intellectual property. According to a venture capitalist, the actual savings from going offshore is more likely to be 25 to 50% rather than the 80 to 90% suggested by a simple salary comparison.[54]

These costs do not include the time costs borne by the workers involved in the home office as well as the offshore office. As mentioned above, the time required for conferencing at the daily handoff between teams can easily run several hours. The time

[51]. Interview, April 1998.
[52]. Interview, August 2004.
[53]. "Global chip design raises promises and challenges," EE Times, January 11, 1999.
[54]. Interview, May 2004.

differences make the handoff occur very early in the day (in India) or late in the day (Silicon Valley). U.S. engineers complained about the amount of time that the daily communications required, since many of them did not think they were given credited by their high-level management for this extra work or for their contribution to the success of the foreign team. In one case, the U.S. engineers told us that they continually saved the offshore team in Bangalore from grave mistakes, and this took a great deal of time that was not considered part of their own job. When we asked the foreign team about the importance of input from the U.S. team, the Indian engineers agreed that the U.S. engineers were critical in evaluating their work and telling them how to do it or correct or improve it.

In some cases, design offshoring can run up against national security barriers. For example, the U.S. government has placed limits on the export of advanced encryption technology. Communications chips that employ such technology are difficult to design offshore. Either the chip design must be compartmentalized, with the encryption block designed only in the United States, or government approval, subject to possible delays, must be obtained in advance.[55]

U.S. MNC design operations in India. Among the top twenty U.S. semiconductor companies, only two (Micron and Atmel) have *not* established a design center in India. This movement to establish design centers in India is quite recent, and for most companies is in a very early stage. Nine of these companies opened their Indian operations since 2004. In 1985 Texas Instruments was the first U.S. company to establish design operations in India. In the mid- to late-1990s, six U.S. companies, including Intel, Motorola (now Freescale), and Broadcom, set up Indian design centers. The size of the operations varies widely, with Intel employing about 3,000 engineers, and smaller companies like Marvell employing fewer than 100.

The training curve for locally-educated engineers can be steep, and the continued expansion of Indian design groups, augmented by a mobile labor pool, has hampered efficiency. In one instance we studied, a chip design project took twice as long to complete as planned.[56] The range of activities carried out in Indian subsidiaries is quite broad, and can include simple parts of the design flow of a mature technology or can include the entire design flow as at TI.

The case of TI India, the most mature of the U.S. design centers in India, shows the potential for the other offshore chip design investments in India to develop over time. Texas Instruments opened an office in Bangalore in 1985 to work on its design automation software for internal use.[57] In 1988, the company added the design of mixed-signal (analog and digital combined) chips. In 1995, TI added design for DSP devices, the company's flagship product line. In 1998, TI India announced that it had taken its first DSP core from specification to working silicon over the preceding 2 years, and integrated a controller with the DSP function for the first time.

In 2003 TI India announced that it had created a highly integrated DSL chip that was the first to market to include significant analog elements on the same chip as the DSP and network processor. During the specification phase, a team of 20 engineers went to

[55]. Interview, December 2004.
[56]. E-mail communications with Indian chip designer, June 2005.
[57]. The following description is based on a compilation of published accounts and the corporate web site.

TI's Dallas headquarters and worked for 3 months with TI system engineers and dealt directly with TI customers about their requirements. The 130nm-linewidth, 13-million-transistor design was completed in India over the next year by a team of 70, worked the first time, and gave rise to eight patent applications for improvements to DSL technology. TI India had 225 U.S. patents as of August 2003.

TI India also develops design library elements, the basic building blocks needed for physical design, for TI's new processes. Although library elements are low-level intellectual property, they are critical inputs to the design process and used throughout TI's R&D infrastructure. Moreover, the designers engaged in library construction are gaining valuable experience with designing for leading-edge process technology.

Since 1999, TI India has won several awards from EDN Asia, a design industry publication, for its chips. In 2004, a very high-performance analog-to-digital converter was touted during an interview by the company's CEO, who mentioned in passing that it had been designed primarily in Bangalore.[58]

However, as is true of fabrication, design offshoring works both ways, and many foreign companies maintain a Silicon Valley or other U.S. design center to take advantage of the high skills and productivity available there as well as have access to U.S. customers. Philips of the Netherlands, for example, bought VLSI Technology, a major ASIC company with over 2,000 employees (about one-third of whom were fab workers), in 1999 for nearly $1 billion.[59] Hitachi Semiconductor has a U.S. design group several hundred strong.[60] Toshiba has a network of seven ASIC design centers around the United States.[61] Even foreign start-ups may need to have a U.S. design team to work with U.S. customers or to access leading-edge analog design skills.

3.5 Location of Semiconductor Engineers

So what is the net employment impact of fabrication and design offshoring? No definitive answer is possible, but we have seen above (Table 1) that government data suggests that the growth of offshoring in recent years has not prevented growth in the industry's U.S. engineering pool.

Data from the Semiconductor Industry Association (SIA), provide further support for this view (see Table 15). The SIA data are based on an annual survey of large- and medium-sized U.S. semiconductor companies, which together represent approximately 80% of the U.S. industry's sales, and then the results are extrapolated to represent all U.S. semiconductor firms.

Although the data may not be strictly comparable from year to year, they can be used to discuss general trends and confirm other data. The total engineering employment at these companies has increased significantly over the period, with the offshore engineering staff growing slightly faster in most years.

The number of engineers located in the U.S. experienced a sharp increase at the end of the 1990s, before the recession caused a slump in employment during the early 2000s.

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[58]. "Texas Instruments collects on split fab strategy bet," EE Times, May 17, 2004.
[59]. "Philips to acquire VLSI Technology for $953 million," Semiconductor Business News, May 3, 1999.
[60]. "Hitachi Forms North America Semiconductor Systems Solutions Unit," Hitachi Press Release, September 2, 1998.
[61]. "Toshiba Expands Soc Design Support Network With Opening Of San Diego Design Center," Toshiba Press Release, November 26, 2002.

Then another sharp increase in U.S. employment is recorded between 2004 and 2005, although the OES engineer data for those two years do not confirm such a trend.[62]

The number of offshore engineers takes a sharp jump in 1998, and again in 2001, and again in 2005. Even with the ups and downs, the percentage of the workforce in the United States tended to hover between 70% to 80% over the 1998 to 2003 period, and then it fell to 66% in 2004-2005. These data indicate a mild shift by these companies in their employment of engineers offshore relative to the United States, which could have a depressive effect on U.S. engineer employment and earnings if it continues.

Table 15: U.S. Semiconductor Engineers By Location, 1997-2005

	1997	1998	1999	2000	2001	2002	2003	2004	2005
U.S.-based Engineers	49,702	46,704	61,856	76,129	72,564	72,860	71,991	66,581	83,167
Offshore Engineers	7,253	19,692	17,446	19,964	27,226	29,813	30,876	34,632	42,193
Total	58,952	68,394	81,301	98,093	101,791	104,675	104,870	103,217	127,365
% in U.S.	87.3%	70.3%	77.9%	79.2%	72.7%	70.9%	69.9%	65.8%	66.3%

Source: David R Ferrell, "SIA Workforce Strategy Overview," ECEDHA Presentation March 2005; 2004 and 2005 data: unpublished SIA survey results provided by Ferrell.

3.6 Semiconductor Industry Country Profiles

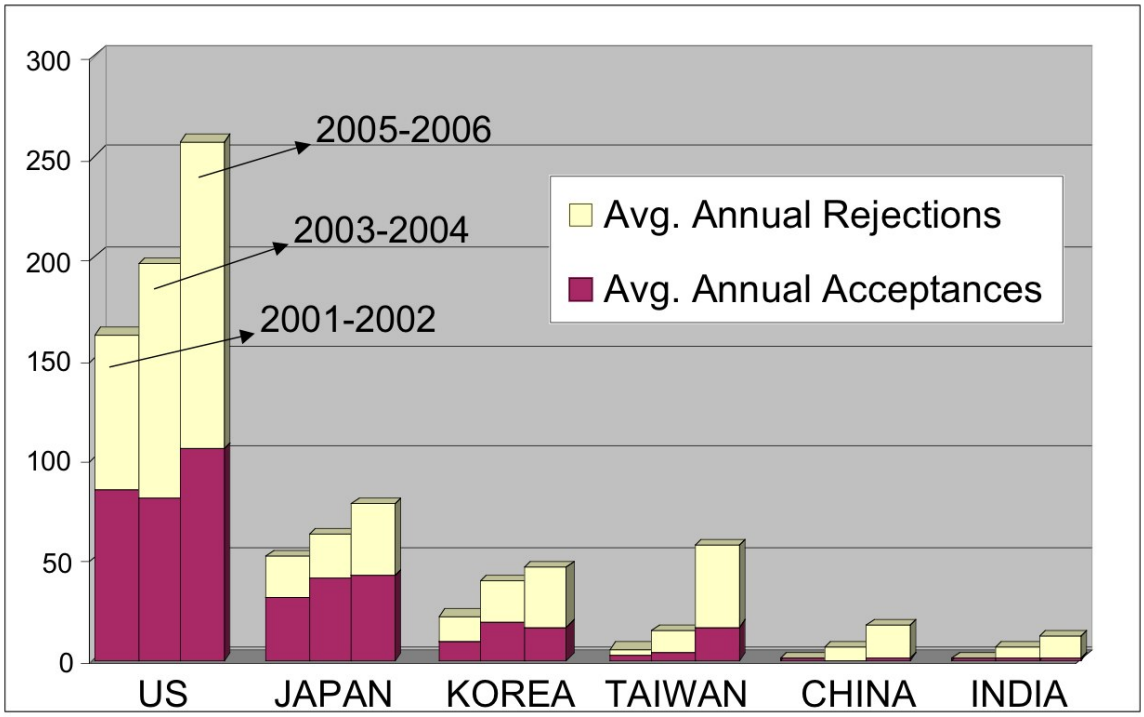
Next we look at the evolution of the chip design sectors in Taiwan, India, and China and compare the technology capability of these countries with the United States. Overall the quality of R&D design engineers, both in the universities and in companies, in Asian countries has been improving, as represented by the submission of papers to the International Solid-State Circuits Conference (ISSCC), which is IEEE's global forum for presentation of advances in chip design (see

Figure 8). Over the 2001 to 2006 period, submissions from China, India, and especially Taiwan increased noticeably. Taiwan's acceptances also increased dramatically, even as the conference's overall acceptance rate fell from 53% to 38%, and we expect

[62] The total for all software and other engineer categories was 73,650 in the May 2004 data and 76,300 in May 2005.

acceptances from India and China will increase in the near future as the quality of their university engineering programs improves

Figure 8: ISSCC Acceptances and Rejections by Country, 2001-2006



Source: tabulated from unpublished ISSCC data

We now turn to an examination of the chip sector in Taiwan, China, and India.

Taiwan has the most well-established semiconductor industry of the three Asian countries. According to Taiwan's Ministry of Economic Affairs, it ranked third (behind the U.S. and Japan) in semiconductor-related patent grants from the U.S. PTO.[63] As discussed above, the foundry model originated in Taiwan in 1987, and three of the top five foundries are located there (Table 11). Taiwan also has successful fabless chip companies, with four companies reporting revenue over $500 million in 2005.[64]

[63] cited in "Taiwan ranks 4th in the world in US patents received," Taipei Times, Oct 17, 2006.
[64] "Data Snapshot," Semiconductor Insights: Asia (FSA), Issue 1, 2006.

Table 16 shows the 2005 value of Taiwan's semiconductor industry output by stage of production. Fabrication, at $18.9 billion, accounts for the largest portion of the $34.8 billion total, followed by chip design at $8.6 billion. Such breakdowns are not possible in most major chip-producing countries because all the stages of production occur within large integrated producers, but Taiwanese companies have embraced the disaggregated business model with only a handful of companies covering multiple parts of the value chain.

Table 16: Taiwan's Semiconductor Industry Value, 2005

	Output Value (US$ billions)	Growth vs 2004
IC design	$8.63	5.8%
Foundry services	$18.9	-3.0%
IC packaging	$5.21	6.4%
IC testing	$2.04	13.0%

Source: IEK-IT IS data, reported in "Taiwan IC production value reached US$34.8 billion in 2005, says government agency," DigiTimes.com, January 19, 2006.

Beginning in the late 1970s, Taiwan benefited from focused government programs and the return of U.S. educated and trained engineers.[65] In 1980, the government created the Hsinchu Science-Based Industrial Park which is still the location of the island's largest concentration of semiconductor firms. Hsinchu is the location of two of Taiwan's leading engineering universities and also home to the government's microelectronics lab, ERSO, which played a pioneering role, including the creation of UMC and TSMC. ERSO undertakes some of Taiwan's most advanced research, and its alumni are encouraged to commercialize technology via start-up companies.

The Taiwanese chip design sector is mostly locally-owned, with a few multinational companies also operating design subsidiaries. Taiwanese companies have embraced the fabless model, with some sixty fabless companies listed on the Taiwan Stock Exchange in December 2004.[66] By comparison, there were about seventy fabless companies listed on NASDAQ at that time. In 2001, the government began a renewed effort (Si-Soft) to improve local chip design capabilities. As part of the program, the faculty teaching chip design more than doubled from 200 in 2001 to more than 400 by 2005.[67]

One advantage for Taiwan's fabless firms is the availability of an important local market, since many Taiwanese companies design, assemble, and procure components for computers, communication equipment, and consumer electronics for world-famous brands, including Hewlett-Packard, Nokia, and Sony. In 1999, 62% of Taiwan's chip design revenue came from local sales.[68]

While Taiwan's design teams were praised in our interviews for their execution, which is a vital trait in an industry where time-to-market is often the difference between profit and loss, Taiwanese companies were mostly fast followers. Ironically, they are locked in to some extent by their reliance on business from the local systems firms, who

[65]. Saxenian (2002).
[66]. FSA "Global Fabless Fundings and Financials Report, Q4 2004".
[67] Chikashi Horikiri, "Taiwan Transforms into IC Development Center," Nikkei Electronics Asia, February 2006.
[68]. Data from Taiwan's Industrial Technology Research Institute cited in Table 5, Chang and Tsai (2002).

are themselves as much as a generation behind the leading-edge technology.[69] As we saw above, Taiwan is second to the U.S. in successful fabless firms. From a U.S. perspective, Taiwanese competition has shortened the market window during which U.S. chip companies can recoup their investments in chips using last-generation technology.

We also saw above that Taiwan depended upon graduate training in the U.S. in the early stage of development of its semiconductor industry. Since the mid-1990s the number of Taiwanese receiving PhDs in engineering has declined steadily, and today few Taiwanese are obtaining graduate training in the U.S. Although graduate training has improved in Taiwan, we heard in our interviews in Taiwan some concern about the declining numbers of returnees from the U.S., who brought with them both graduate training and work experience that imparted management skills as well as practical knowledge.

Taiwan's government has instituted several programs to improve the local design sector, including a plan to train several thousand new design engineers in Taiwan's universities, the creation of an exchange where local chip design houses can license reusable functional blocks, and an incubator where early-stage start-ups can share infrastructure and services.[70] Another initiative aims to attract chip design subsidiaries of major semiconductor companies, with early takers including Sony and Broadcom (a major U.S. fabless company). In 2000, a government research institute created the SoC Technology Center (STC) to design functional blocks that can be licensed to local companies, which is a model Taiwan has used successfully in other segments of the electronics industry. The STC has over 200 engineers, most of whom have a Master's degree or better.[71]

China presents both a major challenge and opportunity for the Taiwanese semiconductor industry. The challenge comes from competition in the foundry and fabless sectors, especially for low-cost designs using older technology, and from competition for engineering talent to work in China and bring with them their knowledge of advanced technology in design and manufacturing. The opportunity comes from the ability to partner with companies in China in the value chain, so that Taiwanese companies can provide high-end design services, and from access to the rapidly growing markets in China. Political issues have been constraining the opportunities for companies to develop partnerships and markets in China, while the companies experience the loss of experienced engineers to Chinese competitors. Currently Taiwan is an important force in the technology development that is occurring in China, in much the same way that the U.S. played a role in the earlier development in Taiwan. Although China seems to be benefiting more than Taiwan from the flows of engineers, capital and business activities between the two countries, this may change over time if Taiwan government policy changes.

China appears to be following a similar pattern to Taiwan: government sponsorship, local access to system firms such as Haier, Huawei, and TCL that are increasingly engaged in world markets, and active involvement of expatriates returning from the United States or experienced engineers relocating from Taiwan.[72]

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[69]. Breznitz (2005).
[70]. "Trends in SOC design unthaw at SOC 2004," EDN, December 9, 2004.
[71]. SoC Technology Center interview, March 2005. "SoC" is a common industry acronym for "system-on-a-chip" meaning a complex semiconductor. integrating multiple functions.
[72]. Saxenian (2002).

In little over a decade, China has developed impressive fabrication capability, with the help of foreign companies (as investors or as technology licensors) and the Chinese government. Table 17 shows the main chip fabs in China, based primarily in Shanghai. The most striking feature is that they are all foundries working under contract rather than companies that design and manufacture their own products. U.S.-based chip companies have few high-profile deals with the China foundries—the major exception being Texas Instruments, which began working with Semiconductor Manufacturing International Corp (SMIC) in 2002 and added a deal to co-develop SMIC's 90nm process in 2004.[73] Executives with U.S. experience have also played key roles. For example CEOs of ASMC and HHNEC had previously worked at AMD.[74]

Table 17: Major Fabs in China, 2006

Company	Fab location	Year entered production	Capacity (wafers per month, 8-inch equivalent)
Advanced Semiconductor Manufacturing Corp (ASMC)	Shanghai	1995	25,000
Shanghai Hua Hong NEC Electronics (HHNEC)	Shanghai	1999	50,000
Semiconductor Manufacturing International Corp (SMIC)	Shanghai, Tianjin, and Beijing	2001	150,000
Grace Semiconductor Manufacturing Corp (GSMC)	Shanghai	2003	27,000
He Jian Technology	Suzhou	2003	42,000
Taiwan Semiconductor Manufacturing Co (TSMC)	Shanghai	2004	15,000; (40,000 planned)

Source: iSuppli data, reported in Cage Chao and Esther Lam, "Despite China-based foundries reporting full utilization rates in 1Q, Taiwan players not overly impressed," Digitimes.com, March 22, 2006

Apart from SMIC, China's foundries have adopted modest growth plans, especially compared to the headline-grabbing predictions of two or three years ago.[75] But there is no question that chip fabrication is firmly established in China and will gradually expand. Although China's fabs pose a growing challenge to the Taiwan foundries, from the perspective of U.S. chip firms they add welcome competition to the market for wafer processing.

A potentially more worrying development for U.S. firms is the emergence of a fabless design sector in China. Since 2003, China claimed to have over 400 chip design firms. Many of these are small, poorly managed and rapidly running through their seed money before they can bring a product to market, while others offer design services

[73] Mark LaPedus, "TI, SMIC sign deal to develop 90-nm technology by Q1 '05," Silicon Strategies, Oct.28, 2004.
[74] Chintay Shih, "Experience on developing Taiwan high-tech cluster," presentation at 4th ITEC International Forum, Doshisha University, June 17, 2006.
[75] Mike Clendenin, "Deflated expectations in China's IC biz," EE Times, August 28, 2006.

rather than their own products.[76] One interviewee, echoed by others, claimed that many, if not most, firms outside the top 10 are engaged in various types of reverse engineering, which is often illegal.[77] Foreign firms are generally reluctant to bring lawsuits for fear of displeasing the authorities and the unlikelihood of winning in Chinese courts, but at least two U.S. companies are suing Chinese rivals in export markets for intellectual property violations.[78]

However the large and growing domestic market provides the opportunity for China's chip design companies to grow and become profitable, so that in the future they may be able to design products for the global marketplace. The local systems firms provide a sizable market for local fabless start-ups. The best design is being done by the local systems firms and a few world-class start-ups headed by U.S. returnees.

China's top 10 chip design firms in 2005 had total revenue of more than $1 billion, $400 million of which is from the Hong Kong-based Solomon Systec, a designer of LCD drivers that was spun off from Motorola in 1999.[79] The next largest firms (Actions, media player chips, $150 million and Vimicro, PC camera image processors, $95 million) had IPOs on NASDAQ in 2005.

The Chinese government has taken many steps in support of chip design firms, some of the largest of whom are state-owned. Measures include tax reductions, venture investing, incubators in seven major cities, and special government projects.[80] A value-added tax preference for domestically-designed chips was phased out under U.S. pressure, and will reportedly be replaced by a WTO-friendly R&D fund, although it has not been announced as of this writing (September 2006).[81]

The return of Chinese nationals with education and work experience has been an important part of China's recent technology development.[82] The returnees provide valuable management experience and connectivity to global networks that will tend to accelerate the pace at which China's chip sector develops.[83] The government maintains statistics on student returnees. In 2003, it was reported that, of 580,000 students that had gone abroad since 1978, 150,000 had returned.[84] These returnees had started 5,000 businesses, including over 2,000 IT companies in Beijing's Zhongguancun Science Park

[76]. Assessment of Byron Wu, iSuppli analyst, reported in "Analyst: China's IC design houses struggling for survival," EE Times, May 20, 2004.
[77]. Interview with a European chip executive, conducted by Elena Obukhova in Shanghai, December 2003.
[78]. See "An offshore test of IP rights," Electronic Business, May 2004; and "SigmaTel Sues Chinese Chipmaker over IP," Electronic News, January 6, 2005.
[79]. Chinese government data cited in Mcallight Liu, "China's Semiconductor Market: IC Design and Applications," Semiconductor Insights: Asia (FSA), Issue 1, 2006 and iSuppli data in Mark LaPedus, "iSuppli lists China's top fabless IC rankings," EE Times, April 21, 2006.
[80]. "Synopsys Teams with China's Ministry of Science and Technology, SMIC," Nikkei Electronics Asia, March 21, 2003; "An Uneven Playing Field," Electronic News, July 3, 2003; "China nurtures home-grown semiconductor industry," EBN, December 8, 2003; "China government to support Solomon Systech, Actions and Silan," DigiTimes, April 14, 2005.
[81]. "China to form R&D fund to replace VAT rebate, says report," EE Times, April 15, 2005.
[82] Saxenian (2002).
[83] "Story behind the Story: Design in China is growing, but not exploding," audiocast by Bill Roberts, Electronic Business, September 1, 2006, http://www.edn.com/article/CA6368425.html?text=%22design+in+china%22#
[84] "More overseas Chinese students returning home to find opportunities," November 16, 2003, http://www.china-embassy.org/eng/gyzg/t42338.htm

(one-sixth the park total).[85] China is working to attract more high-tech returnees with a range of specially-targeted incentives and infrastructure.[86]

China is not yet an important destination for design offshoring by U.S. firms. Of the top twenty U.S. semiconductor companies, a handful have opened design centers in China (compared to eighteen in India) as of June 2006. Most of the Chinese centers are targeting the local market for the time being, and, according to press reports, some are engaged in software or system design rather than chip design *per se*. Concerns over intellectual property protection appear to pose a greater barrier to foreign design activity than in India.[87]

Chip design in China is at an early stage. Its relatively young chip design engineers will steadily build their experience. One factor that favors the development of local design companies is that engineers prefer to work for domestic start-ups and domestic companies rather than MNCs. Many young Chinese engineers, especially returnees, want to take the risk working for an emerging company that may result in great wealth. Some companies, particularly those whose founders include expatriates returning with foreign education and experience, will likely begin to impact global markets by the end of the decade. It is too early to predict the eventual relative importance of domestically-owned and foreign-owned chip design activity, or to predict whether domestic firms will be involved mostly with contract services or with creating and selling their own chips.

Education of semiconductor engineers is also at an early stage. As discussed above, the quality of the engineering graduates varies widely, and few of them have the knowledge and skills to work on advanced technology or for MNCs. Multinational companies, including chip and EDA firms, have been involved with improving engineering education in China, and the government has been actively involved with recruiting world-class engineering professors to Chinese universities. Over time we expect semiconductor engineering education, especially at the graduate level, to continue improving. Returnees from the U.S. and experienced engineers from Taiwan will continue to play an important role in transferring technology to China.

India presents a very different picture than China in the semiconductor industry. India faces benign neglect by the government, a lack of manufacturing for chips and systems, and weaker levels of brain circulation with its U.S.-based expatriates.[88] Unlike Taiwan and China, India has no high-volume chip manufacturing, although as many as five proposals to build a foundry are in various stages of negotiation.[89]

India is estimated to have 120 chip design firms. Indian chip design revenue in 2005 is estimated to be $583 million.[90] Much of this chip design is taking place in foreign subsidiaries, including most of the top 20 U.S. companies and many European companies. This flow of semiconductor engineering talent to multinationals slows down the diffusion of technology to local firms. India has no major fabless companies

[85] "More overseas Chinese students return home," January 1, 2004, http://www.china-embassy.org/eng/gyzg/t57364.htm
[86] Mike Clendenin, "China starting to lure back its best brains," EE Times, January 3, 2002.
[87]. "SIA Pushes Steps to Better IP Protection in China," Electronic News, November 17, 2004.
[88]. Saxenian (2002).
[89]. Russ Arensman, "Move over, China," Electronic Business, March 2006.
[90]. Data from Frost & Sullivan, in Chitra Giridhar, "India design firms as product innovators," Electronic Business, July 18, 2006.

designing chips for sale under their own brand. Domestic chip design companies mainly provide design services, which vary in their capabilities. Local design companies use a time and material-based pricing method, which allocates specific tasks to be carried out within set time lines and is easy to execute, according to an India Semiconductor Association (ISA) study. These companies tend to develop simple subsystems according to customer specifications. The larger independent design services firms are much more sophisticated. They use a fixed price method, are able to provide end-to-end solutions that incorporate in-house proprietary IP, and offer design services across the VLSI design flow.[91] The government is developing policies to support domestic chip design firms.

The foreign chip companies were attracted by Indian engineers' use of English and the successful Indian software sector. Many of the early Indian investments by chip companies were software-focused, writing the microcode that becomes part of the chip. Over time, the Indian affiliates have taken on a bigger role, eventually extending to complete chip designs from specification to physical layout. This transition can happen quite quickly. Intel, for example, opened a software center in Bangalore in 1999, then started building a design team for 32-bit microprocessors in 2002.[92]

The American MNCs are highly dependent upon returnees with advanced degrees from the U.S. to develop new projects in India, since most domestically-trained engineers lack the knowledge of the technology being transferred, lack the management skills required, and also lack knowledge of the entire product cycle. So far MNCs in India have had few instances where design engineers leave to start their own companies, as is often the case in the U.S. However we heard of at least two cases of this occurring over the past two years at one U.S. subsidiary. We also heard that the possibility of leaving a multi-national to start a company is becoming more acceptable among Indians engineers, whose personal motivation is often to help India develop rather than to accumulate great wealth.[93]

Foreign subsidiaries are facing formidable problems in their operations in India, including a very tight labor markets and inadequate infrastructure. As in China, the quality of engineering graduates is highly variable. This is exacerbated in India by the fact that most engineers want to study computer science rather than electronics, and many are not aware of the job opportunities in semiconductors. Graduate education in EE is in its infancy, and doctoral education in the seven major technical universities is not up to U.S. standards. The very low wages paid to professors, the lack of expensive and ever-changing EDA tools, and the difficulty and expense in getting engineering chips fabricated, partly explain the problems in developing world-class graduate education. In addition, India has not attracted returnees to the extent that China has, and so the flow of returnees with graduate degrees is low. The low flow of new domestic graduates and returnees into the EE labor supply, coupled with the need for at least three to five years of experience to be a fully-productive chip designer, has prevented the supply of design engineers from keeping up with the fast-growing demand. As a result, wages for chip designers have been rising rapidly, both at entry level and during the first five years. As mentioned above, salaries after five years of experience are double the entry-level salary.

[91] "Study: Indian design firms prefer time and material model", EE Times, Sept 22, 2006

[92]. "Intel, TSMC Set Up Camps In Developing Asian Markets," WSJ.com, August 30, 2002.

[93] Personal communications in Bangalore, November 2005.

Inadequate infrastructure, especially in Bangalore, also imposes serious problems for chip design centers. The lack of a stable energy supply and lack of office space means that foreign subsidiaries must make substantial investments to provide both offices and electricity. The small, pot-filled roads are gridlocked in Bangalore, and only buses provide mass transit, and so employees spend long hours in commuting. In addition, high-tech companies are spread out over the city, and commuting between companies, or even between company locations, is very time consuming. The housing stock has not kept up with growth, and housing prices and rents have been rising rapidly. Many employees are faced with the choice of living in inadequate housing or living far from work. The housing and schooling problems are especially severe for the returnees from the U.S., who want to replicate the quality of housing and schools their families experienced in the United States. In Bangalore, we were told by several executives that their cost of living was almost as high in Bangalore as in the U.S. because of the high cost of housing and international schools.[94]

The shortage of engineering talent and weak infrastructure is constraining how fast the semiconductor design industry, both for foreign subsidiaries and local companies, can grow in India, especially in Bangalore. Some companies have been moving operations to areas that are not as expensive as Bangalore and have better infrastructure. However the talent shortages still remain, especially for experienced engineers with advanced degrees, since they are attracted to working in Bangalore.

We now look at the outlook for semiconductor engineers in the U.S. and sum up what we know so far about how U.S. companies and engineers have fared as the industry has become more global. Then we briefly look at some key policy issues, and conclude with lessons learned so far.

4. Outlook and Conclusion

The U.S. remains the world leader in the semiconductor industry in terms of market share, development of successful new companies, supply of experienced engineers, and graduate engineering education, and the U.S. is the largest market, both for chip users and end customers. Our competitors, especially Japan, Korea, Taiwan, and the EU, look to the U.S. for lessons in how to foster innovation and emerging companies in the semiconductor industry. Nonetheless, competition from low-cost countries, especially China and India who have rapidly growing and potentially large markets, may pose threats to U.S. companies and engineers in the future.

4.1 Outlook for U.S. Engineers

The job market for U.S. semiconductor engineers shows some strength in employment and earnings growth, but evidence of labor market problems exist, especially for older engineers and for the bottom 10 percent across all education groups. We also observed signs of a decline in the earnings premium for a graduate degree (MS/PhD compared to a BS), and low returns to experience for engineers with graduate degrees. The situation is especially difficult for older engineers, who face rapid skill obsolescence. Experienced design engineers are often forced to work on mature technologies, which pay less. For example, the EE Times 2004 salary survey found that

[94] Personal communications in Bangalore, November 2005.

the average annual salary for U. S. and European engineers skilled at designing for the latest chip process technology was $107,000, whereas engineers designing for the more mature analog technology averaged $87,000.[95]

Results from a regional survey of the Silicon Valley, considered the cradle and creative font of the semiconductor industry, reveal a difficult job climate there. Overall the number of jobs in the Silicon Valley has continually decreased since 2001. Silicon Valley jobs in the semiconductor and semiconductor equipment industries declined 23% between 2002 and 2005, although the average wage rose 12% during the same period, painting a mixed picture of the sector's health.[96]

Perhaps unsurprisingly, industry participants themselves are split on the significance of offshoring for the U.S. job market. A 2004 survey of more than 1,453 chip and board design engineers and managers by EE Times shows that about half saw foreign outsourcing as leading to a reduction in headcount. Qualitative opinions in the survey were also divided, with optimists noting that reduced costs made for a stronger company and a more secure job, while the pessimists bemoaned downward pressure on wages and employment plus a possible loss of intellectual property and, in the long run, industry leadership.[97]

We have observed some movement of design jobs over the business cycle. A wave of design offshoring took place at the height of the dot.com bubble. When the cascading effect of the subsequent downturn reached the semiconductor industry, chip companies cut staff at home. Now that the recovery requires expansion of design operations, chip companies appear to be expanding design operations abroad faster than at home.[98] It is too early to predict where this relative shift in the geographic distribution of employment will find a new equilibrium.

Even experts cannot agree if the U.S. is educating too few engineers and scientists and is facing a shortage.[99] This is partly because economists find it hard to think a shortage exists in a labor market when real earnings are not rising across the board, as is generally the case in the high-tech engineering labor market. Partly this is a reflection of government policies that affect immigration and education of high-tech engineers, which we discuss below.

4.2 Policy Issues

The industry's offshoring has gone well beyond the point where blunt instruments such as trade policy can help engineers without harming companies. Taxes or quotas on traded activities or goods would raise the cost structure of the many companies who have already invested offshore in a wide array of design and manufacturing activities for both the foreign and the domestic chip market.

Policy is thus unlikely to be able to improve the demand side of the labor market, and industry has been active in lobbying for changes on the supply side in the form of

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[95]. "After 10-year surge, salaries level off at $89k," EE Times, August 28, 2003.
[96]. Joint Venture: Silicon Valley Network, "2006 Index of Silicon Valley," available online at http://www.jointventure.org/PDF/Index%202006.pdf. The data are from state unemployment insurance data, which is the basis for the Census data.
[97]. "It's an outsourced world, EEs acknowledge," EE Times, August 27, 2004.
[98]. See, for example, "The perfect storm brews offshore," Electronic Business, March 2004, accessible at www.reed-electronics.com/eb-mag/toc/03%2D01%2D2004/
[99] See for example Richard B., Freeman (2003, 2005); Task Force On The Future Of American Innovation (2005); National Research Council (2000, 2001); William Butz et al (2004).

education and immigration changes. The Winter 2005 newsletter of the Semiconductor Industry Association includes articles such as "Maintaining Leadership As Global Competition Intensifies" by the organization's president and "America Must Choose To Compete" by the outgoing CEO of Intel. One of the main targets of these industry analyses is education. Higher education policies, which reflect both university decisions and government funding, determine the number and country of origin of engineering graduates at all levels.

Government policies regulating immigration, especially the issuance of H-1B (Non-Immigrant Professional) and L-1 (Intra-Company Transfer) visas, have an important impact on the number of foreign engineers engaged in semiconductor and software work. Changes in the policy appear to have had an effect on in-house offshoring. When the number of H-1B visas issued was dramatically cut in 2004 in a delayed response to the recession, many U.S. companies used the opportunity to send foreign nationals with U.S. education and experience back to India and China to help build operations there.

In addition, higher education policies, which reflect both university decisions and government funding, determine the number and country of origin of graduate students at all levels but especially the graduate level. The importance of foreign nationals in our MS and PhD programs in science and engineering has a direct impact on the supply of knowledge workers both in the United States as well as China and India. Foreign graduates of U.S. universities must obtain temporary visas, usually H1-B visas, before they can work in the U.S. after graduation. Legislation is under consideration to provide permanent residency status to foreigners educated in the United States, and hopefully this policy will be implemented soon.

An area of policy that has received less attention is compensation to engineers who are harmed by offshoring. Thanks to the offshoring of chip design, consumers benefit from lower prices and new products (although much of that benefit is received outside the United States), but some of the short-term cost of the offshoring is borne by engineers in particular companies or industry sectors whose companies are restructuring globally. Currently, white-collar workers like chip designers don't qualify for trade-adjustment assistance from the government when their jobs are sent abroad. It would make sense to help these workers with retraining and other forms of assistance that will keep these highly-skilled individuals productive. As Federal Reserve Chair Bernanke remarked, "The challenge for policymakers is to ensure that the benefits of global economic integration are sufficiently wide-shared — for example, by helping displaced workers get the necessary training to take advantage of new opportunities — that a consensus for welfare-enhancing change can be obtained."[100]

Finally, more and better data are needed. As researchers in other industries have noted, more labor market data, both for the U.S. and our trading partners, are needed in order to properly understand offshoring and its effects.[101] National policies affecting education, labor markets, and innovation will continue to be based upon informed speculation.

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[100] Edmund L. Andrews, "Fed Chief Sees Faster Pace for Globalization", *New York Times*, August 25, 2006

[101] See the excellent study by Tim Sturgeon et al (2006).

4.3 How should U.S. engineers respond?

American engineers can and are responding to the impact that the changing labor market is having upon their careers. The highly-rewarded career path of working for one company for one's entire adult life is no longer an option for most engineers, who can expect to work for several firms. In fact, changing jobs is now the way that engineers can develop their careers, both in terms of improving pay and in learning new technologies and skills. Networking with colleagues from one's alma mater and former companies as well as through professional associations is an excellent way to keep up with knowledge about job opportunities as well as to learn about new technologies.

Our advice is to semiconductor engineers is to embrace the mobile labor market and see job change as the way to advance your own development. Choose your next job carefully to improve your skills and learn from experience. Continually stay in touch with your network, and share knowledge with your colleagues about what is happening in the field and about job opportunities. Today's engineers must be in charge of their careers; they can no longer depend upon their employer to provide them with the continual training they need to keep up their skills.

Foreign nationals who are working for U.S. companies can use their networks to develop their careers both in the U.S. and in the home country. Returnees can bargain good salary packages with their U.S. employers, if they are willing to return home for short- or long-term stints. U.S. nationals should go abroad to develop contacts and expertise about specific cultures and regional markets.

Semiconductor engineers are known for their flexibility and ability to solve challenging problems and learn new technologies. The semiconductor industry will remain in continual crisis and change. Chip engineers should use these industry characteristics to their advantage in planning their careers by seeking jobs where they can learn new technology and new markets. To be successful in the industry, an engineer (or manager) must view change as an opportunity rather than a problem.

4.4 Lessons Learned

In its short history, the semiconductor industry has faced continual challenges, usually seen as crises, and has done an extraordinary job of overcoming them, often in innovative ways that were not anticipated. The industry has also continually experienced large swings in demand and prices, and we expect the cyclical nature of the industry to continue, even as the long-term trend is upward. In predicting the future of the industry and in setting policy, we must not extrapolate from the short run, especially during a down turn, since this will not provide the correct basis for making policy, either by governments or by companies.

Macro policies that ensure a strong economy with steady growth are critical to the development of the semiconductor industry, which is harmed by national recessions and by high interest rates.

Government support of higher education, especially graduate education, should be the cornerstone of public policy to support innovation. A strong university system with state-of-the-art graduate training and strong links to companies is critical for innovation in the semiconductor industry. U.S. universities play a central role in educating PhD-level engineers, who are as likely to be from Asia as from the U.S. A company's knowledge

base incorporates the workers' contacts at their former universities as well as at former employers, and these university and professional social networks are an important extension of a firm's formal knowledge. Company awareness of this is critical to ensuring that employees' knowledge is acquired and used, and not just leaked.

4.5. Conclusion

The semiconductor industry is still in the intermediate stages of globalization, which is a complex dynamic process, and policy interventions need to be flexible. At this point it is hard to say what the impact of offshoring will be on the competitive position of the U.S. semiconductor industry, how long it will take for the economy to adjust, and whether the new equilibrium will be acceptable.

Offshoring has provided an important step in the integration of India and China into the global economy. China and India appear to be pursuing different roles vis-à-vis the United States, with the Chinese industry acting more as a more a competitor (e.g. fabless start-ups) and the Indian industry playing a more a complementary role (e.g. design services). Both countries will play an increasingly important role in high-tech industries, both as markets and suppliers. However their ability to move up the technology curve is constrained by lack of graduate education, undeveloped financial systems, and inadequate IP protection, as well as political systems that face severe problems.

We expect the United States to maintain its leadership position in the semiconductor industry, and we expect the industry and its resourceful engineers to continue to find ways to overcome challenges. Modifications in government policies affecting universities, immigration, and workers affected by trade would alleviate some of the labor market problems observed.

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