David J. Allstot

allstot@gmail.com; Office: 541-737-4746; Cell: 541-908-0311

Education

B.S., Engineering Science, University of Portland, 1969
M.S., Electrical and Computer Engineering, Oregon State University, 1974
Ph.D., Electrical Engineering and Computer Science, University of California, Berkeley, 1979

Research Interests

System-on-chip integration of mixed-signal and RF Integrated Circuits

Career Summary

Research Highlights

- > 100 archival journal papers: ~ 50 in *IEEE J. Solid-State Circuits (JSSC)*, ~ 30 in *IEEE Trans. on Circuits and Systems (TCAS)*, 2 in *Proceedings of the IEEE* (Invited), etc.
- > 200 Conference papers: ~20 in *IEEE Intl. Solid-State Circuits Conf. (ISSCC)*, ~15 in *IEEE Custom Integrated Circuits Conf. (CICC)*, ~20 in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, ~30 in *IEEE Intl. Symposium on Circuits and Systems (ISCAS)*, etc.
- >30 books, book chapters and papers reprinted in edited volumes
- 40 Ph.D. Graduates. Several hold academic positions:
  - Dr. Terri S. Fiez, Vice Chancellor for Research and Innovation, University of Colorado
  - Dr. Michael P. Flynn, Prof., University of Michigan
  - Dr. Jianjun Zhou, Prof. and Director, Analog/RF IC Centre, Institute for Microelectronics, Shanghai Jiao Tong University
  - Dr. Bertan Bakkaloglu, Prof. of ECEE, Arizona State University
  - Dr. Jeyanandh Paramesh, Adjunct Professor, Carnegie Mellon University, Research Prof., Southern Methodist University, and Founder and CEO, Spatial Radio Technologies, Inc.
  - Dr. Cameron Charles, Senior Hardware Engineer, Amazon, Inc., and Affiliate Assistant Prof. of EE, University of Washington
  - Dr. Nathan Neihart, Associate Prof. of ECE, Iowa State University
  - Dr. Adam Chu, Adjunct Assistant Prof., University of California at Santa Cruz
  - Dr. Gaurab Banerjee, Associate Prof., Indian Institute of Science
  - Dr. Sankaran Aniruddhan, Associate Prof. of EE, Indian Institute of Technology, Madras
  - Dr. Kuang-wei Cheng, Associate Prof. of EE, National Cheng Kung University, Taiwan
  - Dr. Sudip Shekhar, Associate Prof. of ECE, University of British Columbia, Vancouver, BC
  - Dr. Kristen Naegle (M.S.E.E. UW 2004, Ph.D. MIT 2010), Assoc. Prof. of Biomedical Engineering, University of Virginia
  - Dr. Subhanshu Gupta, Assistant Prof. of EECS, Washington State University
  - Dr. Jinho Park, Adjunct Prof. of EE, Daegu Gyeongbuk Inst. of Science and Technology, Korea
  - Dr. Sangmin Yoo, Assistant Prof., Michigan State University
  - Dr. Rajesh Zele, Professor, Dept. of EE, Indian Institute of Technology, Bombay, and Professor-in-Charge and Director of the IIT Bombay Research Park
  - Dr. Sang-Soo Lee, Adjunct Professor, Dept. of EE, San Jose State University
- Member of U.S. National Academy of Engineering (2020) "For research and commercialization of mixed-mode integrated circuits and systems"
- Fellow of IEEE (1992) "for contributions to the analysis and design of switched-capacitor and analog integrated circuits"
- IEEE W.R.G. Baker Prize Paper Award (1980)
- Darlington Award, *IEEE Circuits and Systems Society (CASS)* (1995, 2010)
- Beatrice Winner Award, *IEEE ISSCC* (1998)
- Best Paper Award, *IEEE Trans. on Biomedical Circuits and Systems* (2015)

- 50-Year Anniversary Author Honor Roll, *IEEE ISSCC* (2003)
- Charles A. Desoer Technical Achievement Award, *IEEE CASS* "for outstanding contributions to mixed-signal and RF integrated circuit design" (2004)
- University Research Award, *Semiconductor Industries Association* "for excellence in research, graduate advising and impact of students on the US Semiconductor industry" (2008)
- Mac Van Valkenburg Award, *IEEE CASS* "for contributions to mixed-signal and RF integrated systems" (2011)
- Meritorious Service Award, *IEEE CASS* "for contributions to mixed-signal and RF integrated systems" (2019)

Teaching and Education Highlights

- Taught ~100 courses on digital, analog and radio frequency integrated circuits
- As Professor of ECE at Oregon State University, conceived, developed and taught the first freshmen design courses ECE 111-112: Introduction to Electrical and Computer Engineering I and II. In 2000 these courses were expanded into the *TekBots* Program
- Developed ~10 new graduate courses including the world's first graduate CMOS Analog IC Design course while an Adjunct Assistant Prof. at Southern Methodist University (1981)
- Loyd Carter Award, College of Engineering, Oregon State University "for Outstanding Undergraduate Teaching" (1988)
- Eta Kappa Nu Outstanding Teaching Award, Dept. of Electrical and Computer Engineering, Carnegie Mellon University (1993)
- Aristotle Award, Semiconductor Research Corporation, "for excellence in graduate advising and impact of graduate students on the US Semiconductor industry" (2005)
- As Chair of the Dept. of Electrical Engineering at UW, led the development and implementation of a new undergraduate "skinny core" curriculum that features flexibility for students with interdisciplinary interests
- John Choma Education Award, *IEEE CASS* "for sustained contributions with global impact on integrated circuits and systems education" (2018)

Research Funding

- ~$40M in research funding from US Government funding agencies (NSF, DARPA), industrial consortia (SRC, NSF Center for the Design of Analog/Digital Integrated Circuits) and high-technology companies (Texas Instruments, Intel, National Semiconductor, Qualcomm)

Professional Service Highlights

- *IEEE*: Member Fellow Committee (2014-15, 2018-); Member Fellow Committee Strategic Planning Sub-Committee (2018-19); Member Awards Board (2016); Chair of Kirchhoff Award Committee (2010-12)
- *IEEE CASS*: Distinguished Lecturer (2000-01, 2018-19); President-elect, President, and Past-president (2008-10): Editor *IEEE TCAS* (1993-95); Assoc. Editor, *IEEE TCAS* (1990-93); Co-General Chair, *IEEE Intl. Symposium on Circuits and Systems* (2001, 2008)
- *IEEE Solid-State Circuits Society*: Distinguished Lecturer (2006-07)
- *IEEE ISSCC*: Member Executive Committee (1996-00); Short Course Organizer (1996-00); Member Technical Program Committee, *IEEE ISSCC* (1994-04)

Most Significant Publications

- D.J. Allstot, R.W. Brodersen and P.R. Gray, "MOS switched-capacitor ladder filters," *IEEE JSSC*, vol. 13, pp. 806-814, Dec. 1978.
  First paper on the design and implementation of high-precision MOS switched-capacitor (SC) ladder filters. The technique has been used in billions of sampled-data signal processing chips
- G.M. Jacobs, D.J. Allstot, R.W. Brodersen and P.R. Gray, "Design techniques for MOS switched-capacitor ladder filters," *IEEE TCAS*, vol. 25, pp. 1014-1021, Dec. 1978.
  *First paper on design theory for MOS SC ladder filters (*1980 *IEEE W.R.G. Baker Prize Award)*
- W.C. Black, Jr., D.J. Allstot and R.A. Reed, "A high-performance low-power CMOS channel filter," *IEEE JSSC*, vol. 15, pp. 929-938, Dec. 1980.
  The first SC filter for PCM telephony in CMOS, which introduced two-stage CMOS operational amplifiers. It set power and performance records and motivated the switch from NMOS to CMOS
- D.J. Allstot and W.C. Black, Jr., "Technological design considerations for monolithic MOS switched-capacitor filtering systems," *Proc. of the IEEE*, vol. 71, pp. 967-986, Aug. 1983.
  Invited comprehensive paper that described design and layout considerations for CMOS SC filters
- D.J. Allstot, S.H. Chee, S. Kiaei and M. Shrivastawa, "Folded source-coupled logic vs. CMOS static logic for low-noise mixed-signal ICs," *IEEE TCAS I*, vol. 40, pp. 553-563, Sept. 1993.
  *Introduced low-noise digital logic techniques for mixed-signal applications with 300X less digital switching noise than CMOS static logic (*1995 *IEEE CAS Society Darlington Award)*
- N.K. Verghese, D.J. Allstot and S. Masui, "Rapid simulation of substrate coupling effects in mixed-mode ICs," *IEEE CICC*, 1993, pp. 18.3.1-18.3.4.
  The seminal paper on CAD substrate noise simulation techniques; it combined discretization of the substrate and RC network reduction using Asymptotic Waveform Evaluation (AWE). This CAD opened a new major research area. Modern CAD tools for mixed-signal IC design use key ideas from this paper
- N.K. Verghese, T.J. Schmerbeck and D.J. Allstot, *Simulation Techniques and Solutions for Mixed-Signal Coupling in IC*. Boston: Kluwer Academic Publishers, 1995.
  The first comprehensive book on substrate noise coupling in mixed-signal IC design included CAD simulation techniques and mitigation strategies at the chip, package and board levels
- M.P. Flynn and D.J. Allstot, "CMOS folding A/D converters with current-mode interpolation," *IEEE JSSC*, vol. 31, pp. 1248-1257, Sept. 1996.
  The first folding and interpolating ADC fully compatible with digital CMOS technology
- J.-J. Zhou and D.J. Allstot, "Monolithic transformers and their application in a differential CMOS RF low-noise amplifier," *IEEE JSSC*, vol. 33, pp. 2020-2027, Dec. 1998.
  The first paper to describe the use of monolithic transformers in CMOS IEEE RFIC design
- B.M. Ballweber, R. Gupta and D.J. Allstot, "A fully integrated 0.5-5.5GHz CMOS distributed amplifier," *IEEE JSSC*, vol. 35, pp. 231-239, Feb. 2000.
  The paper described the first fully-integrated high-accuracy CMOS distributed amplifier. It introduced the parasitic-aware design paradigm wherein substrate and other parasitics are included in the design and optimization processes from the beginning of the design
- S.T. Lee, S.J. Fang, D.J. Allstot, A. Bellaouar, A.R. Fridi and P.A. Fontaine, "A quad-band GSM-GPRS transmitter with digital auto-calibration," *IEEE JSSC*, vol. 39, pp. 2200-2214, Dec. 2004.
  A low-power fully-integrated fast-locking quad-band GSM-GPRS transmitter. It introduced closed-loop PLL up-conversion using a modulated fractional-N synthesizer with digital auto-calibration
- J. Paramesh, R. Bishop, K. Soumyanath and D.J. Allstot, "A four-antenna receiver in 90nm CMOS for beamforming and spatial diversity," *IEEE JSSC*, vol. 40, pp. 2515-2524, Dec. 2005.
  The first fully-integrated CMOS MIMO receiver for beamforming and spatial diversity. A novel Cartesian combiner was introduced, which used vector combinations of variable-gain amplifiers
- X. Li, S. Shekhar and D.J. Allstot, "G_m-boosted LNA and VCO circuits in 0.18μm CMOS," *IEEE JSSC*, vol. 40, pp. 2609-2619, Dec. 2005.
  The g_m-boosted common-gate circuit architecture is disclosed, which broke the link between noise match and input power match so that both can be optimized simultaneously

- S. Shekhar, J.S. Walling and D.J. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE JSSC*, vol. 41, pp. 2424-2439, Nov. 2006.
  Inductive-peaking-based bandwidth extension (BWE) for CMOS amplifiers is described. A critical parameter for optimum BWE is the ratio of driver device drain capacitance to load capacitance. Thus, different techniques are used for different ratios, enabling designs with record BWE ratios of 4.9
- D. Ozis, J.K. Paramesh and D.J. Allstot, "Integrated quadrature couplers and their application in image-reject receivers," *IEEE JSSC*, vol. 44, pp. 1464-1476, May 2009.
  Multi-stage lumped-element quadrature hybrids enhance bandwidth, amplitude and phase accuracies for use in a fully-integrated double-quadrature heterodyne receiver front-end. Measured IRR is > 55 dB over a 200 MHz bandwidth at 5.25 GHz without tuning, trimming, or calibration
- J.S. Walling, S.S. Taylor and D.J. Allstot, "A class-G supply-modulator and class-E PA in 130 nm CMOS," *IEEE JSSC*, vol. 44, pp. 2339-2347, Sept. 2009.
  The first class-G PA in CMOS; it used a class-G modulator with a class-E PA operating in an EER mode
- S. Yoo, J. Walling, E.-C. Woo and D. Allstot, "A switched-capacitor PA for EER/polar transmitters," *IEEE ISSCC*, Feb. 2011, pp. 428-429.
  The first switched-capacitor RF PA in CMOS operates in an EER mode and efficiently amplifies signals with large peak-to-average ratios.
- A.M.R. Dixon, E.G. Allstot, D. Gangopadhyay and D.J. Allstot, "Compressed sensing system considerations for ECG and EMG wireless bio-sensors," *IEEE Trans. on Biomedical Circuits and Systems*, vol. 6, pp. 156-166, April 2012.
  The first paper on the design/performance considerations for integrated compressed-sensing systems

Professional Experience

Positions Held

- Adjunct Professor, Dept. of Electrical and Computer Engineering, Texas A&M Univ. (1/1/2020 -)
- Professor, School of EECS, Oregon State University (2017-)
- Affiliate Professor, Dept. of EE, Univ. of Washington (2013 -)
- MacKay Professor in Residence, Dept. of EECS, UC Berkeley (2013-16)
- Executive Director, Berkeley Wireless Research Center, UC Berkeley (2013-15)
- Visiting Professor, School of EECS, Oregon State Univ. (2012-13)
- Visiting Professor, Dept. of EE, Stanford Univ. (2011-12)
- Professor, Dept. of EE, Univ. of Washington (1999-2012)
- Boeing-Egtvedt Chair Professor, Univ. of Washington (2000-12)
- Chair, Dept. of EE, Univ. of Washington (2004-07)
- Professor, Dept. of ECE, Arizona State Univ. (1998-99)
- Hewlett-Packard Professor, Dept. of ECE, OSU (1995-98)
- Professor, Dept. of ECE, Carnegie Mellon Univ. (1991-95)
- Assoc. Director, CMU/SRC CEDA Center (1991-95)
- Assoc. Professor, Dept. of ECE, CMU (1990-91)
- Assoc. Professor, Dept. of ECE, Oregon State Univ. (1986-90)
- Visiting MacKay Professor, Dept. of EECS, UC Berkeley (1985-86)
- Senior Design Engineer, MOSTEK, Inc., Carrollton, TX (1980-81)
- Adjunct Assistant Professor, Dept. of EE, Southern Methodist Univ. (1980-81)
- Member of Technical Staff, Texas Instruments, Inc., Dallas, TX (1979-80)
- Acting Assistant Professor, Dept. of EECS, UC Berkeley (1979)
- Design Engineer, Tektronix, Inc., Beaverton, OR (1973-75)

Recent Boards and Commissions

- Technical Advisory Board, Shanghai Will Microelectronics (2016 -)

- Technical Advisory Board, Sentons (2012 -)
- Technical Advisory Board, Telegent Systems (now Broadcom) (2009-11)
- Engineering Advisory Council, University of Portland (2007-18)
- Technical Advisory Board, Montage Semiconductor (2006 -)

Honors and Awards

- Member of U.S. National Academy of Engineering (2020)
- *IEEE ISSCC:* Best Evening Session Awards: "Lessons Learned—Great Circuits That Didn't work—(Oops, If Only I Had Known!)" (2019); "SOC: RIP? DOA?" (2003); Outstanding Long Service Award (for outstanding contributions as program committee member 1994-04) (2004); 50-Year Anniversary Author Honor Roll (2003); Outstanding Service Award (for outstanding contributions as short-course chair 1996-00) (2000); Beatrice Winner Award (1998)
- *IEEE CASS*: Meritorious Service Award (2019); John Choma Education Award (2018); Van Valkenburg Award (2011); Desoer Technical Achievement Award (2004); Golden Jubilee Medal (1999); Darlington Best Paper Award: (S. Shekhar, et al.) (2010); (S. Kiaei, et al.) (1995)
- *Semiconductor Research Corp.*: SRC/TXACE 10-Year Anniversary Founder Award (2018); Aristotle Award (2005); Inventor Recognition Award (2003)(1994); First-Place SiGe Design Competition (2002)
- *IEEE Trans. on Biomedical Circuits and Systems*: Best Paper Award (A.M.R. Dixon, et al.) (2015)
- *IEEE RFIC:* Best Student Paper Award: (S. Gupta, et al.) (2011); (K.-W. Cheng, et al.) (2009); (K. Choi, et al.) (2004)
- *Semiconductor Industries Association*: University Research Award (2008)
- *University of Washington, Dept. of Electrical Engineering*: Chair's Award (2007); Outstanding Research Advisor Award (2006)(1999)
- *National Science Foundation:* Research Initiation Award (1987-90); Center for the Design of Analog/Digital Integrated Circuits (CDADIC) Best Project Award (2007)(1998)
- *Oregon State University*: Engineering Academy Distinguished Engineer (2006)
- *IEEE Asia South Pacific Design Automation Conf. (ASP-DAC)*: Best Paper Award (M. Chu, et al.) (2004)
- *Carnegie Mellon University, Dept. of ECE*: Eta Kappa Nu Outstanding Undergraduate Teaching Award (1993)
- *IEEE*: Fellow "for contributions to the analysis and design of switched-capacitor and analog integrated circuits" (1992); IEEE W.R.G. Baker Prize Paper Award (G. Jacobs, et al.) (1980)
- *Oregon State Univ., College of Engineering*: Loyd Carter Award for Outstanding Teaching (1988)
- *Southern Methodist University, Dept. of EE*: Outstanding Teaching Award (1981)
- *Sigma Xi Scientific Research Society* (1978)
- *Intl. Business Machines*: IBM Ph.D. Fellowship (1977-79)
- *Eta Kappa Nu Electrical and Computer Engineering Honor Society* (1976)

Professional Service

- Plenary Co-Chair, *IEEE ISCAS* (2022)
- Editorial Board, *Proceedings of the IEEE* (2020-22)
- President's Advisory Committee, *IEEE CASS* (2020)
- Chair, John Choma Education Award Committee, *IEEE CASS* (2019)
- Member, IEEE Fellow Committee (2014-15, 2018-)
- Member, IEEE Fellow Strategic Planning Sub-Committee (2018)
- Distinguished Lecturer, *IEEE CASS* (2000-01, 2018-19)
- Tutorial Co-Chair, *IEEE ISCAS* (2018)

- Member, *IEEE CASS* Fellow Committee (2016-17)
- Member, Meritorious Service Award Committee, *IEEE CASS* (2007, 2017)
- Member, IEEE Awards Board (2016)
- Member, Mac Van Valkenburg Award Committee, *IEEE CASS* (2018)
- Chair, Mac Van Valkenburg Award Committee, *IEEE CASS* (2016)
- Member, Grievance Board, *IEEE CASS* (2016)
- External Review Committee, Dept. of ECE, Texas A&M Univ. (2016)
- Division I Rep., IEEE Technical Activities Board Awards and Recognition Committee (2012-14)
- Member, Forum Selection and Oversight Committee, *IEEE ISSCC* (2012, 2014-15)
- Chair, Nominations Committee, *IEEE CASS* (2006, 2011)
- Chair, Grievance Board, *IEEE CASS* (2011)
- Chair, IEEE Gustav Robert Kirchhoff Technical Field Award Committee (2010-12)
- President-Elect, President, Past-President, *IEEE CASS* (2008-10)
- Member, IEEE Technical Activities Board (2008-10)
- General Chair, *IEEE ISCAS* (2008)
- Member, IEEE Kirchhoff Award Committee (2007-10)
- Member, Constitution and Bylaws Committee, *IEEE CASS* (2007)
- Distinguished Lecturer, IEEE Solid-State Circuits Society (2006-07)
- Member, Aristotle Award Committee, SRC (2006)
- Member, Nominations Committee, *IEEE CASS* (2005)
- Member, Darlington Best Paper Award Committee, *IEEE CASS* (2005)
- Member, Guillemin-Cauer Best Paper Award Committee, *IEEE CASS* (2005)
- Member, Technical Program Committee, *IEEE Design Automation Conf.* (2002)
- Member, Industrial Pioneer Award Committee, *IEEE CASS* (2002)
- Member, IEEE Solid-State Circuits and Technology Committee (2002)
- General Chair, *IEEE ISCAS* (2001)
- Distinguished Lecturer, *IEEE CASS* (2000-01)
- Co-Chair, IEEE Solid-State Circuits and Technology Committee (1996-98)
- Chair for Short Course, *IEEE ISSCC* (1996-00)
    - 1996: Intro. to Digital Television with C. Heegard, P. Hooijmans, A. King, and T. Chan; 232 Registrants
    - 1997: RF CMOS Circuit Design for Personal Communications Systems with A.A. Abidi, P.R. Gray, T.H. Lee, and M.S.J. Steyaert; 396 Registrants
    - 1998: xDSL Broadband Interactive Communications via POTS with J.A.C. Bingham, J.M. Cioffi, D.A. Johns, and D. Macq; 336 Registrants
    - 1999: Fast Local Area Networks with J.G. Kenney, B. Kim, S. Rao, and B. Razavi; 340 Registrants
    - 2000: Circuits and Devices for RF Wireless Networks with J.D. Cressler, B. Gilbert, L.E. Larson, and A.F. Podell; 368 Registrants
- Member of Executive Committee, *IEEE ISSCC* (1996-00)
- Chair of Special Sessions, *IEEE ISCAS* (1995)
- Member, Technical Program Committee, *IEEE ISSCC* (1994-04)
- Member, Van Valkenburg Award Committee, *IEEE CASS* (1994- 6)
- Member, Technical Program Committee, IEEE Symp. on Low-Power Electronics (1994-97)
- Member, Board of Governors, *IEEE CASS* (1992-95)
- Member, Education Award Committee, *IEEE CASS* (1990-93)
- Member, Technical Program Committee, IEEE Custom IC Conf. (1990-93)
- Assoc. Editor, Analog IC and Signal Processing, Kluwer Academic Publishers (1990 -)
- Editor-in-Chief, *IEEE TCAS* (1993-95)
- Assoc. Editor, *IEEE TCAS* (1990-93)

Publications

Books

1. N.K. Verghese, T.J. Schmerbeck and D.J. Allstot, Simulation Techniques and Solutions for Mixed-Signal Coupling in IC, Kluwer, Boston, 304 pages, 1995. ISBN: 0-7923-9544-1
2. D.J. Allstot, K. Choi and J. Park, Parasitic-aware Optimization of CMOS RF Circuits, Kluwer, Boston, 184 pages, 2003. ISBN: 1-4020-7399-2

Book Chapters; Edited Volumes; Papers in Edited Volumes

1. D.J. Allstot, R.W. Brodersen and P.R. Gray, "MOS switched-capacitor ladder filters," *IEEE JSSC*, vol. 13, pp. 806-814, Dec. 1978; reprinted in Analog MOS IC, P.R. Gray, D.A. Hodges and R.W. Brodersen, Editors, *IEEE Press*, pp. 259-267, 1980. ISBN: 0-87942-142-8
2. G.M. Jacobs, D.J. Allstot, R.W. Brodersen and P.R. Gray, "Design techniques for MOS switched-capacitor ladder filters," *IEEE TCAS*, vol. 25, pp. 1014-1021, Dec. 1978; *ibid*, pp. 267-274. ISBN: 0-87942-142-8
3. D.J. Allstot, R.W. Brodersen and P.R. Gray, "An electrically programmable switched-capacitor filter," *IEEE JSSC*, vol. 14, pp. 1034-1041, Dec. 1979; *ibid*, pp. 315-322. ISBN: 0-87942-142-8
4. D.J. Allstot, S.K. Lui, T.S.-T. Wei, P.R. Gray and R.G. Meyer, "A high-voltage analog-compatible I^2L process," *IEEE JSSC*, vol. 13, pp. 479-483, Aug. 1978; reprinted in Integrated Injection Logic, J.E. Smith, Editor, *IEEE Press*, pp. 307-310, 1982. ISBN: 0-87942-137-1
5. D.J. Allstot, R.W. Brodersen and P.R. Gray, "MOS switched-capacitor ladder filters," *IEEE JSSC*, vol. 13, pp. 806-814, Dec. 1978; reprinted in MOS Switched-capacitor Filters: Analysis and Design, G.S. Moschytz, Editor, *IEEE Press*, pp. 272-280, 1984. ISBN: 0-87942-177-0
6. G.M. Jacobs, D.J. Allstot, R.W. Brodersen and P.R. Gray, "Design techniques for MOS switched-capacitor ladder filters," *IEEE TCAS*, vol. 25, pp. 1014-1021, Dec. 1978; *ibid*, pp. 281-288. ISBN: 0-87942-177-0
7. D.J. Allstot and W.C. Black, Jr., "Technological design considerations for monolithic MOS switched-capacitor filtering systems," *Proc. of the IEEE*, vol. 71, pp. 967-986, Aug. 1983; *ibid*, pp. 368-387. ISBN: 0-87942-177-0
8. D.J. Allstot and K.-S. Tan, "Simplified MOS switched-capacitor ladder filter structure," *IEEE JSSC*, vol. 16, pp. 724-729, Dec. 1981; *ibid*, pp. 427-432. ISBN: 0-87942-177-0
9. D.J. Allstot, R.W. Brodersen and P.R. Gray, "An electrically programmable switched-capacitor filter," *IEEE JSSC*, vol. 14, pp. 1034-1041, Dec. 1979; *ibid*, pp. 449-456. ISBN: 0-87942-177-0
10. G.M. Jacobs, D.J. Allstot, R.W. Brodersen and P.R. Gray, "Design techniques for MOS switched-capacitor ladder filters," *IEEE TCAS*, vol. 25, pp. 1014-1021, Dec. 1978; reprinted in Selected Papers on Integrated Analog Filters: Advances in Circuits and Systems, G. Temes, Editor, *IEEE Press*, pp. 13-20, 1987. ISBN: 0-87942-215-7
11. D.J. Allstot, S.K. Lui, T.S.-T. Wei, P.R. Gray and R.G. Meyer, "A high-voltage analog-compatible I^2L process," *IEEE JSSC*, vol. 13, pp. 479-483, Aug. 1978; reprinted in High Voltage IC, B.J. Baliga, Editor, *IEEE Press*, pp. 135-138, 1988. ISBN: 0-87942-242-4
12. D.J. Allstot, "A precision variable-supply CMOS comparator," *IEEE JSSC*, vol. 17, pp. 1080-1087, Dec. 1982; reprinted in Analog MOS IC, II, P.R. Gray, B.A. Wooley and R.W. Brodersen, Editors, *IEEE Press*, pp. 99-106, 1988. ISBN: 0-87942-246-7
13. G.M. Jacobs, D.J. Allstot, R.W. Brodersen and P.R. Gray, "Design techniques for MOS switched-capacitor ladder filters," *IEEE TCAS*, vol. 25, pp. 1014-1021, Dec. 1978; *ibid*, pp. 159-166. ISBN: 0-87942-246-7
14. D.J. Allstot and W.C. Black, Jr., "Technological design considerations for monolithic MOS switched-capacitor filtering systems," *Proc. of the IEEE*, vol. 71, pp. 967-986, Aug. 1983; *ibid*, pp. 167-186. ISBN: 0-87942-246-7

15. W.C. Black, Jr., D.J. Allstot and R.A. Reed, "A high-performance low-power CMOS channel filter," *IEEE JSSC*, vol. 15, pp. 929-938, Dec. 1980; *ibid*, pp. 213-222. ISBN: 08794224677
16. D.J. Allstot, R.W. Brodersen and P.R. Gray, "Fully-integrated high-order NMOS sampled-data ladder filters," *IEEE ISSCC*, 1978, pp. 82,83,268; reprinted in *Commemorative Supplement of the IEEE ISSCC*, pp. 136,137,153, 1993
17. B.J. Sheu and D.J. Allstot, Guest Editors, *IEEE JSSC*, vol. 28, pp. 191-404, March 1993
18. D.J. Allstot and N.E. Weste, Guest Editors, *IEEE JSSC*, vol. 29, pp. 163-371, March 1994
19. D.J. Allstot and R.H. Zele, "Current-Mode Continuous-Time Filters"; in Analog Circuit Design: Low-Power Low-Voltage, Integrated Filters and Smart Power, R.J. Van de Plassche, W.M.C. Sansen and J.H. Huising, Eds, Kluwer Academic Pubs, pp. 227-235, 1995. ISBN: 0-7923-9513-1
20. D.J. Allstot, B.E. Boser and J.F. Ewen, Guest Eds., *IEEE JSSC*, vol. 31, pp. 1843-2063, Dec. 1996
21. S. Mitra, R.A. Rutenbar, L.R. Carley and D.J. Allstot, "Substrate-aware mixed-signal macrocell placement in WRIGHT," *IEEE JSSC*, vol. 30, pp. 269-278, March 1995; reprinted in Computer-Aided Design of Analog IC and Systems, R.A. Rutenbar, G.G.E. Gielen and B.A. Antao, Editors, *Wiley-IEEE Press*, pp. 461-470, 2002. ISBN:978-0-471-22782-3
22. B.R. Stanisic, N.K. Verghese, R.A. Rutenbar, L.R. Carley and D.J. Allstot, "Addressing substrate coupling in mixed-mode ICs: Simulation and power distribution synthesis," *IEEE JSSC*, vol. 29, pp. 226-238, March 1994; *ibid*, pp. 473-489, 2002. ISBN:978-0-471-22782-3
23. N.K. Verghese and D.J. Allstot, "Computer-aided design considerations for mixed-signal coupling in RF ICs"; *ibid*, pp. 545-554, 2002. ISBN:978-0-471-22782-3
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Ph.D. Degrees

1. Howard C. Yang, *Design Considerations for Fast-Settling Operational Amplifiers*, OSU, Sept. 1989
   - First Position: Senior Design Engineer, National Semiconductor Corp., Santa Clara, CA
   - Now: Chairman and CEO, Montage Technology, Ltd., Shanghai, Adjunct Prof., Hong Kong University of Science and Technology and Adjunct Prof., School of Microelectronics, Shanghai Jiao Tong University
2. Terri S. Fiez, *Analysis and Design of CMOS Switched-Current Filters*, OSU, June 1990
   - First Position: Assistant Prof. of EECS, Washington State University
   - Now: Vice Chancellor for Research and Innovation, University of Colorado
3. Philip Canfield, *Design and Optimization of Gallium Arsenide MESFETS*, OSU, June 1990
   - First Position: Semiconductor Device Engineer, Hewlett-Packard Co.
   - Now: Senior Director of Quality and Reliability, Inphi Corp. (Retired 6/1/2017)
4. Guojin Liang, *Current-Mode Analog and Digital Circuit Design*, OSU, Dec. 1990
   - First Position: Staff Engineer, EXAR Corp.
   - Now: Analog/Mixed-Signal Technology Consultant
5. Sang-Soo Lee, *Simulation of Electro-Thermal Interactions in Integrated Circuits*, CMU, Aug. 1993
   - First Position: Senior Design Engineer, Micro Linear Corp.
   - Now: CEO, Anaflash, Inc., and Adjunct Prof., Dept. of EE, San Jose State Univ.
6. Rajesh H. Zele, *Low-Voltage CMOS Continuous-Time Filters*, CMU, April 1994
   - First Position: Staff Engineer, Motorola, Inc.
   - Now: Professor, Dept. of EE, Indian Institute of Technology, Bombay, India, and Professor-in-Charge and Director of the IIT Bombay Research Park
7. Michael P. Flynn, *High-Speed CMOS Folding and Interpolating Analog-to-Digital Converters*, CMU, April 1995
   - First Position: Member of Technical Staff, Texas Instruments, Inc.
   - Now: Prof., University of Michigan
8. Bertan Bakkaloglu, *Computer Arithmetic Circuits for Fast Eigen-analysis using Matrix Sector Functions*, OSU, June 1995. (Co-advised with Prof. Cetin Koc)
   - First Position: Member of Technical Staff, Texas Instruments, Inc.

- Now: On Semiconductor Professor, Arizona State University

9. Nishath K. Verghese, *Extraction and Simulation Techniques for Substrate-Coupled Noise in Mixed-Signal IC*, CMU, Aug. 1995
   - First Position: Member of Consulting Staff, Cadence Design Systems, Inc.
   - Now: Senior Director of Research and Development, Synopsys, Inc.
10. Ravi Gupta, *Design and Computer-Aided Optimization of RF CMOS Power Amplifiers*, OSU, July 1998
    - First Position: Member of Technical Staff, Maxim Integrated Products, Inc.
    - Now: Senior Director of Engineering, Cypress Semiconductor Corp.
11. Jianjun J. Zhou, *CMOS Low Noise Amplifier Design Utilizing Monolithic Transformers*, OSU, Aug. 1998
    - First Position: Senior Engineer, RF and Analog IC Design Group, Qualcomm, Inc.
    - Now: Professor, School of Microelectronics, Shanghai Jiao Tong University
12. Hiok-Tiaq Ng, *High-Frequency Continuous-Time Filters Employing Multi-Stage Operational Amplifiers*, ASU, Nov. 1999
    - First Position: Design Engineer, Texas Instruments, Inc.
    - Now: Vice-President of Analog Engineering, Aquantia Corp.
13. Hee-Tae Ahn, *Design and Optimization of a Fully-Differential Fully-Integrated Metal-Oxide-Semiconductor Distributed Amplifier*, ASU, July 2000
    - First Position: Principal Engineer, National Semiconductor Corp.
    - Now: Senior Member of Technical Staff, Altera Corp.
14. Douglas R. Beck, *An 8-b, 1.8 V, 20 MS/s Analog to Digital Converter*, UW, Sept. 2002
    - First Position: Lead Network Engineer, Sony Computer Entertainment
    - Now: Chief Software Scientist, NaturalPoint, Inc.
15. Kiyong Choi, *Parasitic-aware Design and Optimization of CMOS RF Power Amplifier*, UW, July 2003
    - First Position: Senior Design Engineer, Marvell Semiconductor, Inc.
    - Now: Director, SK Hynix Memory Solutions
16. Jinho Park, *Fully-integrated CMOS Ultra-wideband Amplifier Design using Parasitic-aware Optimization Technique*, UW, 2003
    - First Position: Senior Design Engineer, Marvell Semiconductor, Inc.
    - Now: CEO, Terrasquare, Inc. (acquired by GigOptix, Inc.) and Adjunct Prof. of EE, Daegu Gyeongbuk Inst. of Science and Technology
17. Sher Jiun Fang, *CMOS Frequency Conversion Techniques for WCDMA*, UW, Aug. 2003
    - First Position: RFIC Design Engineer, Texas Instruments, Inc.
    - Now: Principal Engineer, Qualcomm, Inc.
18. See Taur Lee, *Quad-band GMSK Transmitter*, UW, Aug. 2003
    - First Position: RFIC Design Engineer, Texas Instruments, Inc.
    - Now: Director of Design, Qualcomm, Inc.
19. Waisiu Law, *Digital Calibration of Non-Ideal Pipelined Analog-to-Digital Converters*, UW, Nov. 2003. (Co-advised with Prof. Ward Helms)
    - First Position: President, Scrupulous Design, Inc.
    - Now: General Manager, Hangzhou SDIC Microelectronics Co.
20. Taeik Kim, *A CMOS Tunable Transmission Line Phase Shifter and Voltage-Controlled Oscillator for Wireless Communications*, UW, March 2004
    - First Position: Senior Analog/RF IC Designer, Freescale Semiconductor
    - Now: Principal Engineer and Project Leader, Samsung Electronics
21. Xiaoyong Li, *Low Noise Design Techniques for Radio Frequency IC*, UW, July 2004
    - First Position: Senior Engineer, Qualcomm, Inc.

- Now: Assoc. Prof., School of Microelectronics, Shanghai Jiao Tong University

22. Hossein Zarei, *Smart Antenna Phase Shift Network Architectures and Circuits*, UW, Aug. 2004
    - First Position: Senior Analog Design Engineer, Freescale Semiconductor
    - Now: Principal Analog/ RFIC Circuit Designer, SaberTek, Inc.
23. Adam Chu, *Phase-Shifting Techniques for Wireless Beamforming Transmitter Applications*, UW, Dec. 2005
    - First Position: Senior RF Design Engineer, Intel Corp.
    - Now: Senior Member of Technical Staff, Integrated Device Technology, Inc., and Adjunct Assistant Prof. of ECE, UC Santa Cruz
24. Dicle Ozis, *Image-Reject Receiver Architecture for Radio Frequency IC*, UW, May 2006
    - First Position: Senior Staff Engineer, Telegent Systems, Inc.
    - Now: Principal Analog and RF IC Design Engineer, Analog Devices, Inc.
25. Sankaran Aniruddhan, *A Fast-Locking Frequency Synthesizer for GSM Base-stations in 180nm CMOS*, UW, June 2006
    - First Position: Senior Engineer, RF-Analog Division, Qualcomm, Inc.
    - Now: Associate Prof. of EE, Indian Institute of Technology, Madras
26. Gaurab Banerjee, *Desensitized CMOS Low Noise Amplifiers*, UW, Aug. 2006
    - First Position: Staff Scientist, Intel Corp.
    - Now: Associate Prof., Indian Institute of Science
27. Jeyanandh K. Paramesh, *CMOS Multi-Antenna Receivers: Architectures and Circuits*, UW, Aug. 2006
    - First Position: Post-Doctoral Research Associate in EE, UW
    - Now: Adjunct Professor, Carnegie Mellon University, Research Prof., Southern Methodist University, and Founder and CEO, Spatial Radio Technologies, Inc.
28. Cameron Charles, *A Calibrated Phase and Amplitude Control System for Phased-Array Transmitters*, UW, Nov. 2006
    - First Position: Assistant Prof. of ECE, University of Utah
    - Now: Senior Hardware Engineer, Amazon, Inc., and Adjunct Assistant Prof. of EE, University of Washington
29. Yi Tang, *Digitally-Assisted Sigma-Delta ADCs for Scaled CMOS Technology*, UW, Nov. 2007
    - First Position: Senior Engineer, Qualcomm Research Center, Qualcomm, Inc.
    - Now: Senior Staff Engineer, Qualcomm Research Center, Qualcomm, Inc.
30. Nathan Neihart, *Circuits for Reduced Coupling in Multiple Antenna Transceivers*, UW, Aug. 2008
    - First Position: Assistant Professor of ECE, Iowa State University
    - Now: Assoc. Professor of ECE, Iowa State University
31. Charles T. Peach, *An 11.1 mW 42 MS/s 10 b ADC With Two-Step Settling in 0.18 μm CMOS*, UW, Aug. 2008
    - First Position: Sr. Analog Circuit Designer, Impinj, Inc.
    - Now: Sr. Director of IC Design, Lumotive LLC, Bellevue, WA
32. Jeffrey S. Walling, *Efficiency Enhancement and Linearization of CMOS Power Amplifiers and Transmitters*, UW, Dec. 2008
    - First Position: Assistant Prof. of ECE, Rutgers University
    - Now: Principal Engineer, Qualcomm, Inc.
33. Sudip Shekhar, *Wideband Frequency Synthesizers*, UW, Dec. 2008
    - First Position: Research Scientist, Intel Laboratories, Intel Corp.
    - Now: Associate Prof. of ECE, University of British Columbia
34. Kuang-Wei Cheng, *Low Power CMOS Receiver For GPS Applications*, UW, May 2009
    - First Position: Senior Research Engineer, Singapore Institute of Microelectronics
    - Now: Associate Prof. of EE, Taiwan National Cheng Kung University

35. Subhanshu Gupta, *A CMOS Direct-RF Sampling Band-Pass ΣΔ Receiver with Integrated QPLL for Software-Defined Radio Applications*, UW, Dec. 2010
    - First Position: Staff Design Engineer, MaxLinear, Inc.
    - Now: Assistant Prof. of EECS, Washington State University
36. Sangmin Yoo, *A Switched-capacitor Power Amplification Technique*, UW, May 2011
    - First Position: Staff Engineer, Qualcomm, Inc.
    - Now: Assistant Prof., Michigan State University
37. Daibashish Gangopadhyay, *Compressed Sensing Analog-to-Digital Converters for Biomedical Applications*, UW, Nov. 2011
    - First Position: Senior Design Engineer, Marvell Semiconductor, Inc.
    - Now: Senior Analog and Mixed Signal Architect, Apple Inc.
38. Parmoon Seddighrad, *Digitally-scalable Transformer-combining Power Amplifier Techniques*, UW, Dec. 2011
    - First Position: Research Scientist, Intel Corp.
    - Now: Senior Platform Architect, Intel Corp.
39. Karthik Natarajan, *A Robust Power-Scalable Transmitter Architecture for Wireless Body Area Networks*, UW, Sept. 2012
    - First Position: Senior RF/Analog Design Engineer, Intel Corp.
    - Now: Same
40. Anna Dixon, *Understanding the Practical Limitations of Applying Analog Compressed Sensing Systems to ECG Acquisition*, UW, Nov. 2012
    - First Position: Staff Scientist, Gryphon Scientific
    - Now: Research Scientist, Sensors and Electron Device Directorate, Army Research Laboratories, Adelphi, MD

Post-Doctoral Associates

1. Dr. Jianjun Guo, UW, Jan. 2003 - Aug. 2003
    - First Position: Research Engineer, General Electric Global Research
    - Now: Vice President of Engineering, FMI Medical Systems, Solon, OH
2. Dr. Jeyanandh Paramesh, UW, Aug. 2006 – Dec. 2006
    - First Position: Assistant Prof. of ECE, Carnegie Mellon University
    - Now: Adjunct Professor, Carnegie Mellon University, Research Prof., Southern Methodist University, and Founder and CEO, Spatial Radio Technologies, Inc.
3. Dr. Jeffrey S. Walling, UW, Jan. 2009 - Feb. 2011
    - First Position: Assistant Prof. of ECE, Rutgers University
    - Now: Associate Prof. of ECE, Univ. of Utah
4. Dr. Sangmin Yoo, UW, June 2011 - Sept. 2011
    - First Position: Staff Engineer, Qualcomm, Inc.
    - Now: Assistant Prof., Michigan State University

M.S.E.E. Degrees

1. Xi (Robert) Jin, *Determination of Impurity Levels in MBE Samples using Photoluminescence Techniques*, OSU, June 1987. (Co-advised with Prof. John Arthur)
    - First Position: Design Engineer, Integrated Device Technologies, Inc.
    - Now: Senior Principal Engineer, Montage Semiconductor, Inc.
2. Pee Kong Or, *Modeling of Subthreshold Current in GaAs MESFET and the Design of Voltage Reference Circuit*, OSU, Dec. 1987
    - First Position: Design Engineer, Sharp Microelectronics, Inc.
    - Now: Senior Staff Component Design Engineer, Intel Corp.

3. John J. Yang, *A High-Swing CMOS Operational Amplifier Topology*, OSU, Feb. 1988
   - First Position: Senior Design Engineer, National Semiconductor Corp.
   - Now: Senior Staff Design Engineer, Marvell Semiconductor, Inc.
4. Tianchen (Albert) Liu, *CMOS Analog Design using a Digital Gate Array*, OSU, April 1988
   - First Position: Product/Test Engineer, Sharp Microelectronics Technology, Inc.
   - Now: Vice-President of Business Development, Montage Technology, Ltd.
5. Chong Yu, *A High-Swing Class-AB CMOS Operational Amplifier*, OSU, April 1988
   - First Position: Senior Design Engineer, Micro Linear Corp.
   - Now: Senior Member of Tech. Staff, Maxim Integrated Products, Inc.
6. Shin (Michael) D. Jen, *Operational Amplifier Compensation Using Doublet Decompression for Switched-capacitor Circuits*, OSU, April 1988
   - First Position: Senior Engineer, Intel Corp.
   - Now: Device, Integration, Quality and Reliability Manager, Intel Corp.
7. Steven C.F. Lam, *Analytical Model of GaAs MESFET Output Conductance with Frequency- and Temperature-Dependent Parameters*, OSU, April 1988
   - First Position: Senior Design Engineer, Micro Linear Corp.
   - Now: Design Engineering Manager, Marvell Semiconductor, Inc.
8. Shu-Ing Ju, *Design of a GaAs Monolithically Integrated Optical Receiver Amplifier*, OSU, May 1988
   - First Position: Senior Design Engineer, National Semiconductor Corp.
   - Now: Principal Engineer, Texas Instruments, Inc.
9. Seung-Han Ahn, *A Chopper-Stabilized CMOS Operational Amplifier*, OSU, May 1988.
10. Ravindra U. Shenoy, *A CAD Noise Model for Chopper-Stabilized Switched-capacitor Filters*, OSU, June 1988
    - First Position: Senior Design Engineer, National Semiconductor Corp.
    - Retired
11. William Jiang, *CMOS Differential Line Driver Circuit Technique*, OSU, April 1989
    - First Position: Design Engineer, Advanced Micro Devices, Inc.
    - Now: Design Manager, Intel Corp.
12. Daniel K. Shum, *Model and Design of a CMOS Phase-Locked Loop*, OSU, June 1989
13. James E. Hansen, A Time-Multiplexed Switched-capacitor Circuit for Neural Network Applications, OSU, June 1989
    - First Position: Senior Design Engineer, Magnavox Electronics Systems Co.
    - Now: Senior Design Engineer, Broadcom Limited, Ft. Collins, CO
14. Bor (Vincent) Lee, *An MOS Switched-Current Biquadratic Filter*, OSU, Oct. 1989
    - First Position: Design Engineer, National Semiconductor Corp.
    - Now: Staff Engineer, Ikanos, Inc.
15. William G. Gazeley, *A Study of the Temperature Dependence of DC Current-Voltage Characteristics of AlGaAs/GaAs Heterojunction Bipolar Transistors with Application to Bandgap Voltage Reference Sources*, OSU, Oct. 1989
    - First Position: Analog/Mixed-Signal Design Engineer, NCR, Inc.
    - Now: Pixel Optics Development Engineer, Aptina Imaging, Inc.
16. Ringo Lee, *Distortion Analysis of CMOS Switched-Current Filters*, OSU, Oct. 1989
17. Mahmoud Abu-Dayeh, *Folded Cascode Operational Amplifier Analysis*, OSU, DEC. 1989
    - First Position: Staff Design Engineer, National Semiconductor Corp.
    - Now: Vice President of Engineering, NVIDIA Corp.
18. Ayse G. Yesilyurt, *A Digitally-Programmable Switched-Current Filter*, OSU, March 1990
    - First Position: Senior Design Engineer, Micro Linear Corp.
    - Now: Staff Design Engineer, Qualcomm, Inc.

19. Paul Lao, *Current Feedthrough Cancellation Techniques for CMOS Switched-Current Filters*, OSU, Aug. 1990.
20. Rajesh Zele, *Fully Differential Current-Mode CMOS Circuits and Applications*, OSU, Aug. 1990.
    - First Position: Staff Engineer, Motorola, Inc.
    - Now: Professor, Dept. of EE, Indian Institute of Technology, Bombay, India, and Professor-in-Charge and Director of the IIT Bombay Research Park
21. Cindy L. Botelho, *A Universal CMOS Current-Mode Operational Amplifier*, OSU, Dec. 1990
22. Vivek Subramanian, *Switched-Current Logic for Digital Circuit Design*, OSU, Feb. 1991
    - First Position: Design Engineer, National Semiconductor Corp.
    - Now: Senior Director, Western Digital Corp.
23. David Y.W. Young, *A Switched-Current Feedthrough Cancellation Technique*, OSU, Feb. 1991
    - First Position: Senior Design Engineer, Advanced Micro Devices, Inc.
    - Now: Venture Partner, BlueRun Ventures, Menlo Park, CA
24. Jung Sheng Hoei, *High-accuracy Switched-Current Filter Design*, OSU, May 1991
    - First Position: Design Engineer, National Semiconductor Corp.
    - Now: Principal Architect, Micron Technology, Inc.
25. Nishath K. Verghese, *Simulation of Substrate-Coupling Effects in ICs*, CMU, May 1993
    - First Position: Member of Consulting Staff, Cadence Design Systems, Inc.
    - Now: Senior Director of Research and Development, Synopsys, Inc.
26. Hiok-Tiaq Ng, *Low-Power Digital Circuit Techniques*, CMU, May 1994
    - First Position: Design Engineer, Texas Instruments, Inc.
    - Now: Vice President of Analog Engineering, Aquantia Corp.
27. Rohit Mittal, *Design and Implementation of Low-Power High-Speed Backward Equalizer Circuits for Magnetic Read-Channel Applications*, CMU, May 1995
    - First Position: Senior Staff Engineer, Micro Linear Corp.
    - Now: Director of Engineering, Intel Corp.
28. John Musa, *Creating and Benchmarking an Analog Tool Flow in the Cadence Environment*, CMU, May 1996. (Co-advisor)
    - First Position: Analog Design Engineer, Wireless Business Unit, Texas Instruments, Inc.
    - Now: Chief Executive Officer, Vortxx Semiconductor
29. Wenjun Su, *Design Of High-Speed Low-Power Analog CMOS Decision Feedback Equalizers*, OSU, July 1996
    - First Position: Design Engineer, Rockwell Semiconductor Systems, Inc.
    - Now: Senior Staff Engineer, Qualcomm, Inc.
30. Anping Liu, *A Trimmed Bandgap Reference Voltage Circuit Design*, OSU, Dec. 1996
    - First Position: Design Engineer, Silicon Systems, Inc.
    - Now: Senior Staff Engineer, Qualcomm, Inc.
31. Ning Li, *A Photodetecting Device That Rejects Ambient Light*, OSU, Feb. 1997
    - First Position: Analog Design Engineer, Medtronic, Inc.
    - Now: Principal Design Engineer, Qualcomm, Inc.
32. Yihai Xiang, *Design of High-Speed Adaptive Parallel Multi-Level Decision Feedback Equalizer*, OSU, Feb. 1997
    - First Position: Senior Design Engineer, Conexant Systems, Inc.
    - Now: President and CEO, ZettaMemory, Ltd.
33. Priya Parthasarathy (Nadathur), *Optimum Quantization for Adaptive Loops in MDFE*, OSU, Feb. 1997 (Co-advised with Prof. Jack Kenney)
    - First Position: Electrical Engineer, Motorola Mobile Devices Technology Office
    - Now: Embedded Firmware Engineer, Amano McGann, Inc.

34. Hairong Gao, *Design of High-Speed Summing Circuitry and Comparator for Adaptive Parallel Multi-Level Decision Feedback Equalization*, OSU, June 1997
    - First Position: Analog Design Engineer, DataPath Systems, Inc.
    - Now: Senior Analog Design Engineer, Microsoft, Sunnyvale, CA
35. Richard Lewison, *Low-Power Sigma-Delta Conversion Techniques for PWM Applications*, OSU, July 1997
    - First Position: Mixed-Signal ASIC Design Engineer, Hewlett-Packard Co.
    - Now: Co-founder and Mobile Applications Developer, Yogi Light
36. Alexander E. Smith, *High Speed Analog Circuit Design Using the Heterostructure Field Effect Transistor*, OSU, Sept. 1997
    - First Position: Member of Technical Staff, Maxim Integrated Products, Inc.
    - Now: Senior Member of Technical Staff, Maxim Integrated Products, Inc.
37. Ramzin Ziazadeh, *Design of High Performance Operational Amplifiers using an Embedded Compensation Technique*, OSU, Dec. 1997
    - First Position: Design Engineer, National Semiconductor Corp.
    - Now: Design Manager, Texas Instruments, Inc.
38. Brett Forejt, *Power Amplifier Design in Digital CMOS Processes*, OSU, Dec. 1997
    - First Position: Design Engineer, Texas Instruments, Inc.
    - Now: Distinguished Member Technical Staff, Texas Instruments, Inc.
39. Brian M. Ballweber, *Design and Computer Aided Optimization of a Fully Integrated CMOS RF Distributed Amplifier*, OSU, Nov. 1998
    - First Position: Wireless Design Engineer, Motorola, Inc.
    - Now: Sr. Principal Electrical Design Engineer, Cypress Semiconductor Corp.
40. Hiok-Hion Ng, *A Fractional-N Phase-Locked Loop Frequency Synthesizer Model for Noised-Shaped and Randomized Frequency Switching*, ASU, Sept. 1999
    - First Position: Staff Design Engineer, DataPath Systems, Inc.
    - Now: Principal Member of the Technical Staff, AMD, Inc.
41. Kiyong Choi, *Design and Optimization of a Class-E Power Amplifier Using Simulated Annealing Techniques*, ASU, Nov. 1999 (Ph.D. July 2003)
    - First Position: Senior Design Engineer, Marvell Semiconductor, Inc.
    - Now: Senior Design Engineer, Qualcomm, Inc.
42. Prashant Mangalvedkar, *High Linearity Switched-capacitor Filter*, ASU, May 2000
    - First Position: Mixed-Signal Design Engineer, Texas Instruments, Inc.
    - Now: Lead Designer, Intersil Corp.
43. Wern M. Koe, *Correlated Double Sampling Technique to Reduce Non-Linearity in Operational Amplifier for Switched-Capacitor Applications*, ASU, July 2000
    - First Position: Member of Technical Staff, Texas Instruments, Inc.
    - Now: Senior RFIC Design Engineer, Global Foundries, Inc.
44. Robert B. Roze, *Class AB-D-G Line Driver for Central Office Asymmetric Digital Subscriber Line Systems*, UW, Aug. 2001
    - First Position: Mixed-Signal Design Engineer, Texas Instruments, Inc.
    - Now: Senior Design Engineer, Broadcom Limited, Ft. Collins, CO
45. Jaynie Shorb, *A Resonant Pad Design for Narrowband Radio Frequency (RF) CMOS Applications*, UW, Aug. 2002
    - First Position: Analog Design Engineer, Zilog, Inc.
    - Now: Principal Design Engineer, Broadcom Corp.
46. Adam Chu, *A Fully Integrated Quadrature LC Oscillator for Applications in the Unlicensed National Information-infrastructure Frequency Band*, UW, Oct. 2002
    - First Position: Senior RF Design Engineer, Intel Corp.

- Now: Senior Member of Tech. Staff, Integrated Device Technology, Inc.

47. Sankaran Aniruddhan, *Low Phase-Noise CMOS Voltage-Controlled Oscillator Design using Lateral Bipolar Transistors*, UW, June 2003
    - First Position: Senior Engineer, Qualcomm, Inc.
    - Now: Assistant Prof. of EE, Indian Institute of Technology, Madras
48. Charles T. Peach, *A 200 Msample/s, 68dB SFDR, Double-Sampled, Pipelined Analog-to-Digital Converter in CMOS*, UW, Aug. 2003
    - First Position: Senior Engineer, Impinj, Inc.
    - Now: Same
49. Srinivas Kodali, *Multi-layered Inductor Structures: Design, Modeling and Applications*, UW, March 2004
    - First Position: Design Engineer, Analog Devices, Inc.
    - Now: Vice President, Fidelity Investments, Boston, MA
50. Kristen Neagle, *Design of a 10GHz CMOS Transmit/Receive Switch*, UW, July 2004
    - First Position: Ph.D. Candidate, Dept. of Biological Engineering, MIT, Cambridge, MA
    - Now: Assoc. Prof. of Biomedical Engineering, University of Virginia
51. Sudip Shekhar, *Bandwidth Extension Techniques: Theory and Applications*, UW, March 2005
    - First Position: Research Scientist, Intel Laboratories, Intel Corp.
    - Now: Associate Prof. of ECE, University of British Columbia
52. Allan Ecker, *Adaptive Online Calibration for MASH Sigma-Delta ADCs Using On-Chip Simulated Annealing*, UW, June 2005
    - First Position: Design Engineer, Tektronix, Inc.
    - Now: Affiliate Assistant Prof. of EE, University of Washington
53. Dan Nicholson, *Design Considerations for Highly Linear CMOS Low Noise Amplifiers*, UW, July 2005
    - First Position: Design Engineer, Boeing Corp.
    - Now: Senior Hardware Design Engineer, EndLess Computing, Inc.
53. Jeffrey S. Walling, *Theory and Application of Spiral Transformers for Silicon-based IC*, UW, July 2005
    - First Position: Assistant Prof. of ECE, Rutgers University
    - Now: Associate Prof. of ECE, University of Utah
54. Naureen Banani, *Evaluation of pH Sensing Techniques for Barrett's Esophagus*, UW, July 2006. (co-advised with Prof. B. Otis)
    - First Position: Product Development Engineer, Intel Corp.
    - Now: Chief of Staff for Custom-Logic ASIC Engineering, Intel Corp.
55. Subhansu Gupta, *Modeling Techniques for Continuous-Time Sigma-Delta Modulators*, UW, Nov. 2006 (Ph.D. Dec. 2010)
    - First Position: Member of Technical Staff, MaxLinear, Inc.
    - Now: Assistant Prof. of EECS, Washington State University
56. Arezou Khatibi, *Design of a 200 MHz Continuous-time Bandpass Filter with Frequency and Q Tuning using Adaptive Filtering Technique*, UW, Dec. 2006
    - First Position: Design Engineer, Qualcomm Inc.
    - Now: Senior Staff Engineer, Qualcomm Inc.
57. Heng-Chia (Gordon) Hsu, *Slow-Wave Coplanar Waveguides for mm-wave CMOS Applications*, UW, May 2008
    - First Position: Analog Design Engineer, Novatek Corp.
    - Now: Senior Analog Design Engineer, Realtek Semiconductor Corp.
58. Karthik Natrajan, *A Second-order Quadrature Bandpass Sigma Delta Modulator for Low-IF Applications*, UW, Aug. 2008

- First Position: RF/Analog Engineer, Intel Corp.
- Now: Senior RF/Analog Engineer, Intel Corp.

59. Eum Chan (Wayne) Woo, *Wide Tuning Range CMOS Ring Oscillator Design Considerations for Nanometer Scale Technology*, UW, Aug. 2009
    - First Position: Analog Design Engineer, Telegent Systems
    - Now: Principal RFIC Designer, Energous Corp.
60. Yongdong (Andrew) Chen, *Analog Chirp Fourier Transform for High-Resolution Real-Time Wideband RF Spectrum Analysis*, UW, June 2011
    - First Position: RFIC Design Engineer, Broadcom, Inc.
    - Now: Ph.D. Candidate in EE, University of Washington
60. Christopher J. Mandic, *A Chopper Stabilized Low-Noise Neurological Amplifier*, UW, July 2012
    - First Position: Electrical Design and Analyst Engineer, Boeing Research and Technology
    - Now: Product Development Engineer, Intel Custom Foundry, Intel Corp.
61. Kevin Park, *Compressed Sensing ICs for Bio-Sensor Applications*, UC Berkeley, May 2014
    - First Position: Design Engineer, Oracle, Inc.
    - Now: Same
62. Brian Wang, *9.7-ENOB SAR ADC for Compressed Sensing*, UC Berkeley, May 2014
    - First Position: Research and Development Electrical Engineer, Agilent Technologies, Inc.
    - Now: Same
63. Xinping Zhang, *DSP Chip of Compressed Sensing Algorithm for Bio-Sensor Application*, UC Berkeley, May 2014
    - First Position: Design Engineer, Advanced Micro Devices, Inc.
    - Now: Same
64. Jun Kwang Oh, *A Robust Compressed Sensing IC for Bio-Signals*, UC Berkeley, May 2014
    - First Position: Ph.D. Candidate in Mechanical Engineering, UC Berkeley
    - Same
65. Zhiyang Song, *Ring-Amplification Technique for Bio-Signal LNA Designs*, UC Berkeley, May 2015
    - First Position: CPU Digital Design Engineer, Intel Corp.
    - Now: Same
66. Guanpeng Zhi, *Low-Noise Amplifier in Switched-capacitor Ring Amplifier with Thermal Noise Cancellation*, UC Berkeley, May 2015
    - First Position: Digital Design Engineer, Oracle, Inc.
    - Now: Same
67. Jonghun Kwak, *A Low-Noise Amplifier for Electrocardiogram Signals*, UC Berkeley, April 2015
    - First Position: Software Engineer, TmaxSoft, Inc.
    - Now: Same
68. Pavan Kumar Ramakrishna, *Energy-efficient OTA Architectures using Load-pole Cancellation*, OSU, Feb. 2019
    - First Position: Associate Engineer, Qualcomm India Private Limited
    - Now: Engineer, Qualcomm Atheros, Inc.
69. Brendan Onn Lim Yong, *A Fully-integrated Bio-potential Low-noise Amplifier Utilizing Capacitance Multipliers*, OSU, March 2019
    - First Position: Senior Design Engineer, AMD, Inc.
    - Now: Same
70. Nayaran Bhagirath Thota, *Efficient Deep Learning Methods for Biomedical Applications*, OSU, Dec. 2019
    - First Position: TBD
    - Now: Same

71. Yu-Wen (Julia) Kuo, *Low Voltage Miller Frequency Compensation for CMOS Operational Amplifiers*, OSU, June 2020
    - First Position: Mixed-Signal Design Engineer, Texas Instruments, Inc. (Aug. 2020)
    - Now: Same
72. Chaiyanut Aueamnuay, *Miller Compensation of Two-stage Operational Amplifiers Using gm/Id Design Techniques*, OSU, June 2020
    - First Position: TBD
    - Now: Same